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Spike Leakage and Burnout of Silicon PIN Diode Microwave Limiters

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Microwave limiters are used to protect sensitive electronics from damage due to exposure to high levels of rf radiation. The two major limitations to the operation of PIN diode limiters are spike leakage, power transmitted before limiting action begins, and damage to the limiter itself due to high power. A combined theoretical and experimental study of spike leakage and burnout has been made for silicon PIN diodes. The diodes ranged in intrinsic-level thickness from 0.5 to 50 μm. Thin diodes, emphasized in this study, have little spike leakage but are damaged at relatively low power. Thick diodes withstand very high powers but have large spike leakage. Although qualitative agreement between the calculations and measurements is excellent, there are important areas of quantitative disagreement. Reasons for the disagreement are suggested. The computer program DIODE, used for the calculations, is described, as are the methods used in the experimental measurements. Useful comparisons have also been made of dc transients and of the forward-biased rf conductivity of the PIN diodes. Suggestions for further work are made.

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1. Introduction

Microwave limiters are used to protect sensitive electronics from damage due to exposure to high levels of rf radiation. The most common application of limiters is to protect the radar receiver from damage from its own transmitter. Gas tubes, usually called T-R tubes, but now beginning to be called receiver protectors (RP's), are commonly used for this purpose. However, there is a delay in the breakdown of a gas into a low-impedance plasma which performs the limiting function. RF energy is transmitted through the RP during this turn-on delay; this phenomenon is termed spike leakage. PIN (positive-intrinsic-negative) diodes were introduced to reduce the spike leakage for increasingly sensitive receivers. PIN diode limiters are also used extensively as the sole limiter in many systems.

PIN diode limiters are high-impedance devices when subject to very low-power rf signals. Thus, when these limiters are placed between the signal and ground, little loss of power is observed. This loss is termed insertion loss. To minimize insertion loss at high frequencies, the unbiased diode capacitance must be kept low. This limits the area of the diode and requires low doping in the intrinsic region of the diode.

When the rf power applied to a PIN diode exceeds approximately 10 mW, the forward RMS voltage (~0.7 V) is sufficient to cause an appreciable forward current to flow. This reduces the diode impedance and begins the limiting action. An ideal PIN limiter would continue to limit (i.e., transmit a constant power) at this level as the applied power increased indefinitely. However, the real life limiter has many deviations from the ideal. The main purpose of this report is to understand and, when possible, to reduce these limitations.

A first limitation of the PIN diode limiters is the presence of spike leakage. Figure 1 illustrates spike leakage. The energy in the spike is small compared to the gas plasma limiter, but is a risk factor to sensitive electronics especially when wide intrinsic region diodes are used. Spike leakage, which is essentially a transit-time phenomenon, is discussed in section 6.

After the spike leakage transient is complete, the limiter would ideally continue to transmit a constant power. This power, which is also shown in figure 1, is termed flat leakage. The flat leakage power is usually plotted

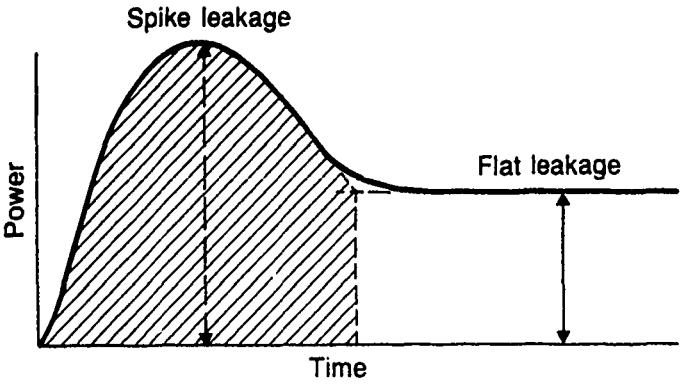


Figure 1. Spike leakage is initial transient power passing limiter before it is turned on. Shaded area indicates energy in the spike.

against the input power to characterize a limiter. This characterization is illustrated in figure 2. Maximum spike leakage power can also be plotted in this manner. As shown in figure 2, all real limiters have a maximum isolation; i.e., the limiter's transmitted power becomes a fixed fraction of the input power. The region between the initiation of limiting and the region of maximum isolation is termed the plateau region. In reality, most limiters have a plateau with appreciable slope. This is a second limitation of a real limiter as compared to the ideal. The limiter characteristic (plateau and maximum isolation regions) is the topic of section 7.

A third and most important limitation of real limiters is that they are also subject to damage. Limiting action is a result of the power absorbed and reflected by the limiter. Fortunately, the drop in impedance by the limiter causes most of the incident power to be reflected by the limiter and thus reduces the absorbed power. Damage thresholds for limiter diodes are discussed in section 8.

The HDL computer program DIODE, used in the limiter calculations, is described briefly in section 2. A general overview of the experimental method and the diodes tested is given in section 3. Video, or dc, pulses are helpful in understanding the turn-on and turn-off transients that are present in rf signals. The forward current-voltage characteristics are also useful in successfully modeling limiters. Section 4 compares calculated and measured video pulse transients and forward characteristics. Because it avoids certain limitations in both calculations and in measurements, the forward biased rf conductivity of PIN limiters allows a better comparison between calculations and measurements than the unbiased state. The limiter under forward bias is the subject of section 5. A general discussion of limiters and the overall HDL diode program makes up section 9. Conclusions are made in section 10, together with suggestions for future work.

There is fairly extensive literature on PIN diode limiters. Garver [1] provides a full chapter on PIN diode limiters, including eight references. Other basic limiter properties are discussed by Watson [2]. The paper by Leenov [3] is still referenced extensively today. High power switching, with limiter

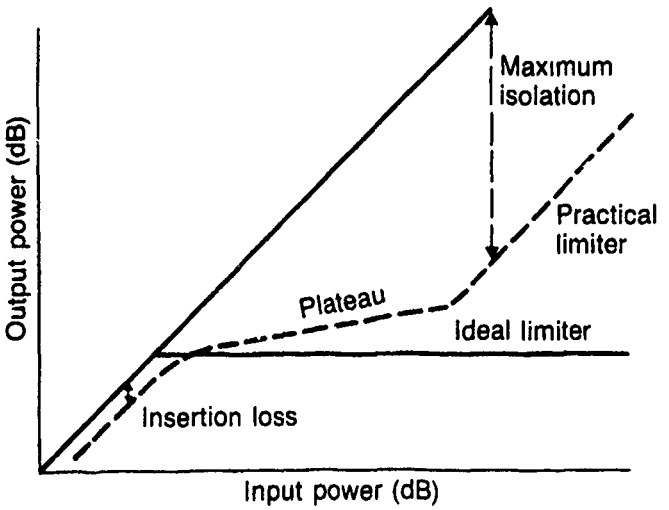


Figure 2. Flat leakage (output power) plotted as a function of input power for ideal and practical limiter, showing plateau region of latter.

implications, was discussed by Caulton et al [4]. Hiller and Caverly [5] provide a modern extension of this paper. There is much useful practical limiter information in the trade literature, for example, a paper on thermal properties of limiters [6].

Our work differs from these earlier works in two basic areas:

(1) This work emphasizes thin I-region devices because we desire low spike leakage levels.

(2) We include the charges in the P-I and the I-N junction regions since, for thin devices, these charges represent a significant percentage of the stored charge in the device.

2. Computer Program DIODE

The computer program DIODE was used in the calculations for this report. A fairly detailed description of DIODE may be found in HDL-TR-1978 [7]. A user's manual for DIODE is now in preparation [8].

Features of the DIODE Program

DIODE is primarily a program to study avalanche and space-charge effects in reverse-biased semiconductor diodes. There are limits on the program's utility for studying the forward-biased diodes. Most important, the boundary conditions are different under the two bias conditions. Therefore, when unbiased rf excitation is being simulated, the forward and reverse half-cycles must be calculated in separate computer runs. Usually, space-charge-free conditions are assumed for the initial conditions of the forward-biased half cycle. That means that the mobile charges are everywhere set equal to the fixed charges. An improved program would calculate the actual partial depletion prevailing with no current flow. However, within the limitations stated above, the use of full depletion conditions from a reverse-bias half-cycle run, as initial conditions for a forward-bias half-cycle calculation, results in waveforms with minor differences from the comparable space-charge-free results.

At the end of the forward half-cycle there is a distribution of stored (electron and hole) charges in the diode. These stored charge distributions form the initial conditions for the reverse biased half-cycle calculation.

The external circuit used in DIODE is shown in figure 3. The capacitance shunting the diode is useful for simulating the finite risetimes of the experimental voltage sources. We plan to modify the present external circuit to include an inductance and resistance in the diode leg to simulate the measured diode lead inductance and the base and contact resistance of the diode.

Mainly because of the circuit RC time constant, the actual diode voltage is delayed in phase from the applied rf voltage. Therefore, the initial voltage across the diode is delayed in phase from the applied voltage in accordance with that calculated during the previous half cycle. This adjustment does have an appreciable effect on the forward half-cycle results, since it effectively reduces the length of the forward half-cycle.

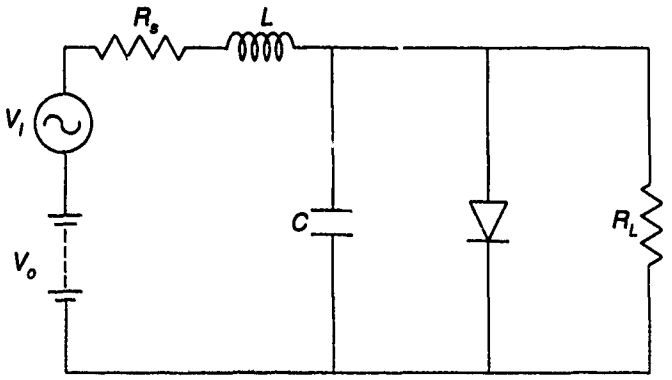


Figure 3. Circuit used in DIODE calculations.

For stability in calculations, the time step chosen must be less than the dielectric relaxation time, which is inversely proportional to the material conductivity. This precludes fully simulating the highest doping in the P and N regions without excessive computer cost. This limitation is important mainly in failing to compute the full stored charges at high currents, in the intrinsic region as well as in the junction regions.

Recombination Rates

The recombination lifetime also has a strong influence on the amount of charge stored in the forward half-cycle and in the recovery time of the reverse half-cycle. A high recombination rate has a stabilizing effect on the calculations. Sometimes calculations have been made with high recombination rates and the stored charges are extrapolated to the higher values expected for more realistic recombination rates.

The recombination rate, $R_R' = dn/dt = dp/dt$, is calculated [7] in DIODE by

$$R_R' = R_R \left(np - n_i^2\right)/n_i \,, \tag{1}$$

where n_i is the intrinsic density, n is the electron density, p is the hole density, and R_R is the recombination parameter used in DIODE. For cases where the majority doping level greatly exceeds the intrinsic level, the minority lifetimes for electrons, τ_n, and holes, τ_p, are found [7] to be

$$\tau_n = n_i/R_R p_o \text{ and } \tau_p = n_i/R_R\, n_o \,, \tag{2}$$

where n_o and p_o are the majority carrier densities. For intrinsic material, the lifetime, τ_i, may be determined as follows. For an initial density of excess carriers of Δ, i.e., $n(o) = p(o) = n_i + \Delta$, where $n(t)$ and $p(t)$ are the time-dependent values, equation (1) becomes

$$d\Delta/dt = -R_R\left[(n_i + \Delta)^2 - n_i^2\right]/n_i \,,$$

which, for small Δ, becomes

$$d\Delta/dt = -2\, R_R\, \Delta \,,$$

whose solution is

$$\Delta(t) = \Delta(o) \exp\left(-2\, R_R\, t\right) \,; \tag{3}$$

therefore, $t_i^{-1} = 2R_R$. Sze [9] gives the recombination lifetime in ideal intrinsic silicon as 2.5×10^{-3}s. Therefore, R_R for ideal intrinsic silicon is 200 s^{-1}. For gold-doped material, R_R is greater.

The ionization coefficients and material parameters used in these calculations were the same as in HDL-TR-1978 [7], except for the low field mobilities. A hole mobility of 400 $cm^2/V \cdot s$ and an electron mobility of 1200 $cm^2/V \cdot s$ was used in this report.

3. Experimental Measurements

3.1 Diodes Used in Experimental Measurements

The PIN diodes used in the experimental measurements, made for HDL by Alpha Industries, Woburn, MA, were fabricated with varying intrinsic region thicknesses from 0.5 to 50 μm. The diodes had a zero bias junction capacitance of approximately 0.3 pF. The diodes were packaged in two types of packages. The first batch received was packaged in pill-prong-type packages (Alpha package 023). These packages had fairly large parasitics, so a second batch of "improved" diodes made from the same wafers or similar substitutes was packaged in a 50-Ω stripline package (Alpha package 375).

The package parasitics of the pill-prong diodes were found to have a significant effect on some of the diode measurements. Therefore, they were measured and are shown in figure 4. These parasitics were measured with the use of two packages without PIN diodes: one with the bond wires connected from one prong to the other creating a shorted package and another left open circuited. The capacitance of the open-circuit package was measured on a capacitance meter to be 0.18 pF. The shorted package was placed in series on a 50-Ω microstrip line, and scattering parameter (S_{21}) measurements were made on a network analyzer from 0.01 to 2 GHz.

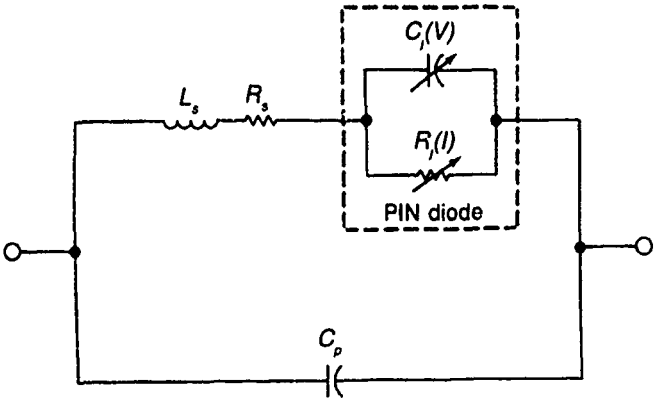


Figure 4. Circuit model of packaged PIN diode.

$C_j(V)$ = junction capacitance
$R_j(I)$ = junction resistance
R_s = series resistance = 0.5 Ω
L_s = series inductance = 3 nH
C_p = package capacitance = 0.18 pF

Assuming that $R_j = 0$, $C_j = 0$, and $C_p = 0.18$ pF and using the circuit model in figure 4, the S_{21} response was used to calculate the series inductance L_s and resistance R_s. They were determined to be 3 nH and 0.5 Ω, respectively. The insertion loss of the 50-Ω stripline package was measured up to 18 GHz to be no greater than 1 dB; therefore, it was concluded that no significant parasitics existed.

3.2 Forward Current and Voltage Measurements

The test setup for measuring the forward current and voltage waveform discussed in section 5 is shown in figure 5. CW rf is applied to a reverse biased diode; then the diode is pulsed with dc in the forward direction during which the rf voltage and current is monitored. Typical current and voltage measurements are shown in figure 13 (see p 18). Because of the availability of only one 6-GHz bandwidth (BW) oscilloscope, the voltage and current traces were taken with two separate pulses; therefore, the phase information between the current and voltage is lost. For these measurements to be accurate, the diodes had to be mounted in a holder with low parasitics, as shown in figure 6. The voltage on the diode was monitored using a high-frequency voltage probe. The current was calculated from the voltage measured across the 2-Ω disk resistor.

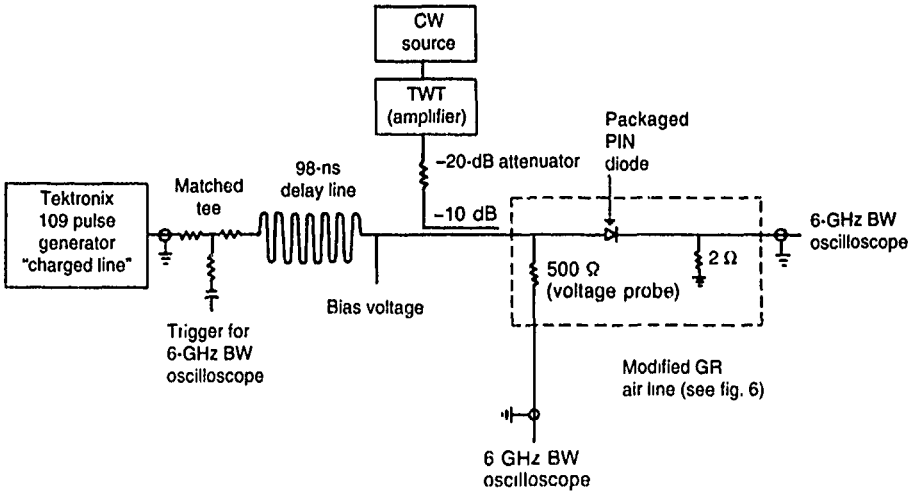


Figure 5. Experimental setup for measuring forward current and voltage waveforms of PIN diodes.

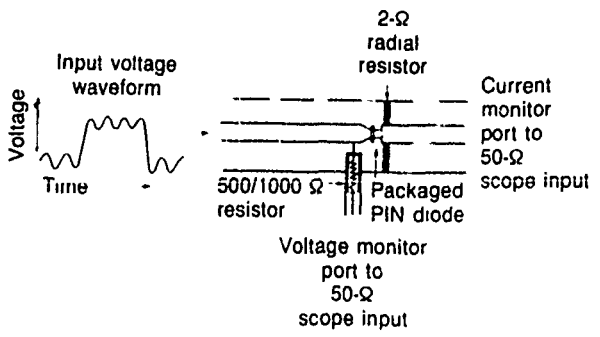


Figure 6. Modified General Radio (GR) 50-Ω air line used to make voltage and current measurements on PIN diode.

3.3 Spike Leakage Measurements

The measured spike leakage data shown in figures 19 and 20 (see p 22) were taken using the experimental setup shown in figure 7. The 1.5-ns risetime input rf pulse was generated with a cw source modulated by fast PIN diode switches and then amplified using a traveling wave tube (TWT). The input power was monitored with calibrated crystal detectors and a 1-GHz BW oscilloscope. The output power was monitored with either a crystal detector or fed directly into a 6-GHz BW oscilloscope.

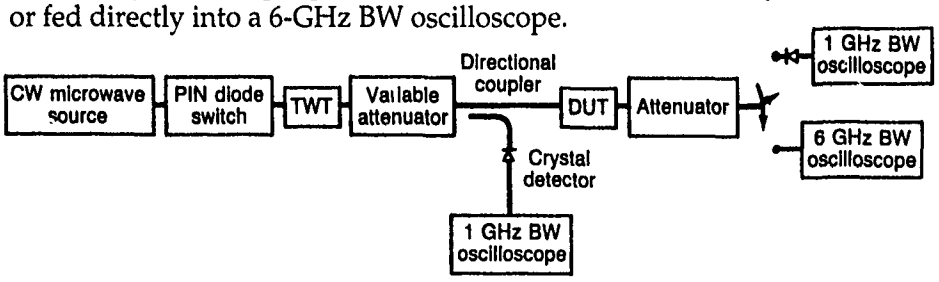


Figure 7. General experimental setup for measuring diode limiter response.

3.4 Video Pulse Measurements

The video pulse measurements were performed with a sample holder similar to figure 6, except the voltage monitor port consisted of a Tektronix P6010 10× probe (input resistance equal to 500 Ω). The probe was positioned as close to the diode package as mechanically possible to minimize the overshoot effects of traveling waves on the mismatched transmission line. All video pulse measurements used PIN diodes in the Alpha 023 pill-prong package or equivalent.

The risetime of both the current and voltage channels was less than 1 ns. The voltage and current signals were measured with either Tektronix 7A19 or 7A26 vertical plug-ins in a 7104 mainframe. The excitation was provided by a Tektronix type 109 "charged line" pulse generator.

4. DC Forward Bias Switching

It was shown in HDL-TR-2057 [10] that the forward-biased dc (video pulse) turn-on transient was useful in predicting the frequency dependence of the diode rf forward half-cycle current and voltage waveforms. A second and verifying example is shown in HDL-TR-2124 [11] for a diode of a different width. Further, the dc steady-state current-voltage characteristic is dependent on the doping profile and the recombination lifetime, among other parameters. Thus, agreement between measured and calculated dc current-voltage characteristics increases confidence in the diode properties (e.g., doping profile and lifetime) used for the rf limiter calculations.

A comparison of the experimental and calculated forward-biased turn-on transient of a 2-μm PIN diode is shown in figure 8. The measurements were performed in a coaxial insertion unit similar to figure 6. Largely because of the probe inductance and oscilloscope capacitance, ringing is observed in the measurements shown in figure 8. Reducing the circuit inductance reduced the overshoots. The measured pulse fit well with calculations for an induc-

tance of 2.5 nH and a capacitance of 40 pF in the circuit of figure 3. Also shown in figure 8 are the transients obtained with $L = 0.1$ nH and $C = 1$ pF, as might be obtained with a very-fast-risetime pulse and oscilloscope.

After a few tens of nanoseconds at most, the measured forward voltage and current become essentially constant, neglecting thermal effects. It is not cost effective to reach complete equilibrium for large numbers of computer calculations. Therefore, the calculated data are termed quasi-equilibrium. A comparison of the measured and calculated characteristics for 2- and 10-μm diodes is shown in figure 9. The agreement is very good for the 2-μm diode and also for the 10-μm diode when the manufacturer's doping profile, obtained from the capacitance-voltage measurements, was used. Doping profiles used in the calculations are shown in figure 10 for the 2- and 10-μm diodes.

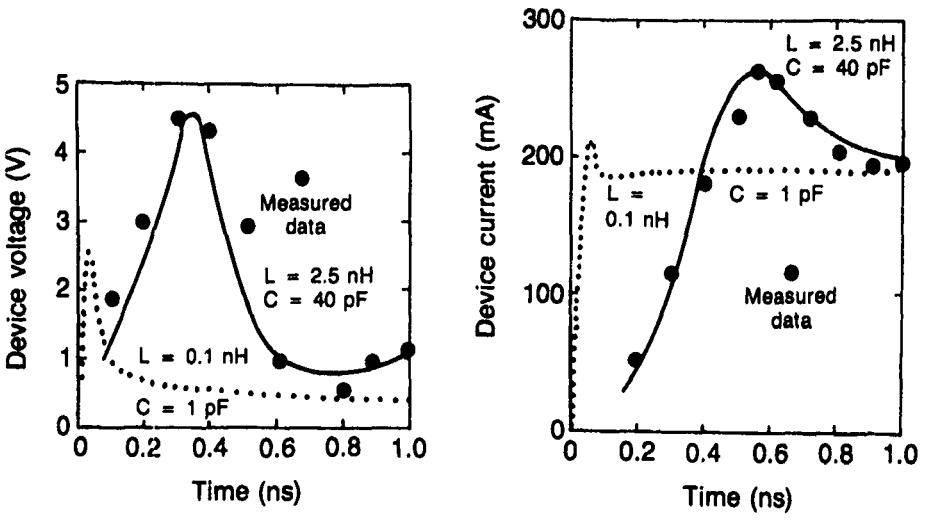


Figure 8. Comparison of measured and calculated forward turn-on voltage and current transients for 2-μm diode.

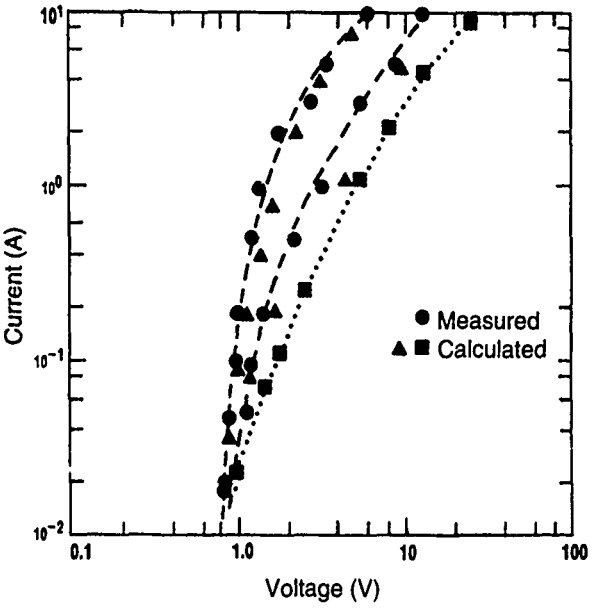


Figure 9. Comparison of measured forward-bias current voltage characteristics with calculated characteristics for 2- and 10-μm diodes. For 10-μm diode, squares indicate an ideal PIN, while triangles indicate measured doping profile results.

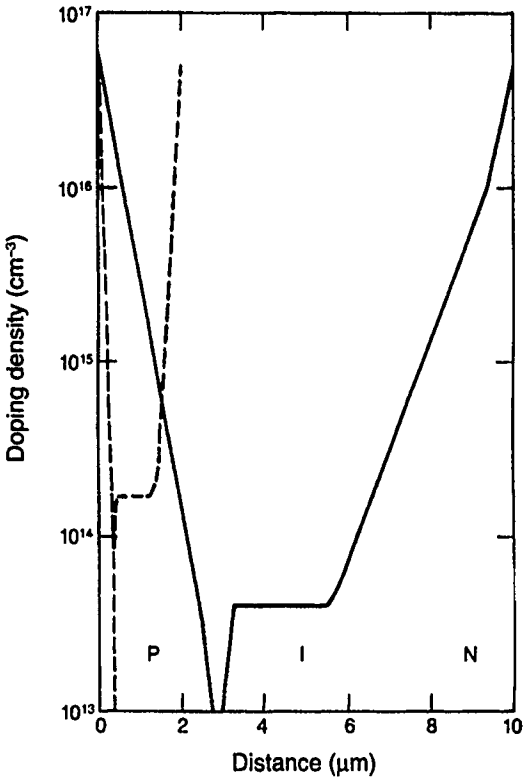


Figure 10. Doping profiles used in calculations, based on capacitance versus voltage measurements of 2- and 10-μm-width diodes.

Examples of both carrier density and electric field plots as a function of distance at selected times for "ideal" PIN diodes are provided elsewhere [10 (fig. 10), 11 (fig. 3)]. Similar plots for the forward half-cycle of an rf oscillation are found in section 6 of this report. In all cases the field is maximum in the central I region. At the boundaries, the field is negative. The negative fields are needed to offset carrier diffusion down the steep carrier gradients. The resulting potential is known as the built-in potential of a junction diode. Since, as explained in section 2, the maximum doping profile used in calculations is less than that used in actual diodes, the built-in potential is also calculated to be less than the true built-in potential. Therefore, the calculated voltages, as in figure 9 for example, have been corrected as follows. If the maximum doping level for calculations is $1 \times 10^{17} cm^{-3}$ as compared to an actual doping of $1 \times 10^{20} cm^{-3}$, then the uncalculated portion of the built-in voltage at each junction must result from a density difference of 10^3 carriers. Since 0.026 V (kT/e at room temperature) results from an exponential-folding of carriers, and ln(10) = 2.303, the extra built-in potential in this case is

$$2 \times 3 \times 2.3 \times 0.026 = 0.36 \text{ V},$$

where the factor of 2 appears since two junctions are involved, and the factor of 3 comes from the three decades of density difference.

At small applied voltages, the maximum p and n region doping levels that can be simulated are limited by persistent negative fields in those regions, which halt the calculations. For high applied voltages, the maximum doping levels must be high enough to keep the boundary fields near zero; otherwise, the calculated voltage is too high. Experience indicates that for valid calcu-

lations the maximum doping level must be several times the plasma density in the center of the I region. This problem is less severe with rf excitation because the low-field-producing instabilities are moving.

The dc turn-off transit or recovery time has also been studied by both calculations and measurements. This switching transient has been widely studied [12], but usually at low power for narrow base diodes. Some results of reverse switching-transient calculations are given in section 16 of HDL-TR-1978 [7]. These early calculations showed that the duration of the switching transients depended strongly on the duration of the forward pulse for an unexpectedly long time. Traditionally, reverse switching has been studied by reverse pulsing a forward-biased diode. This method cannot be used to study the effect of the forward pulse duration; moreover, this method causes much greater heating of the diodes, affecting recovery. By forward pulsing a reverse bias diode, we can determine the effect of the forward pulse length. Figure 11 shows measured recovery times for three diode widths as a function of the forward pulse width. The time for the current to drop to one-half its maximum was chosen as the recovery time. The reverse recovery time was found to increase for higher forward currents and to decrease with higher reverse voltages. Direct comparison of calculated recovery times is precluded, for the long recovery times measured, because of computer cost and other limitations. However, qualitative agreement has been obtained on dependencies on PIN diode widths, forward current levels, reverse bias levels, and forward pulse widths. Figure 12 shows the calculated current transients for reverse switching of a 10-μm diode for selected forward plasma (current) levels.

Many of the physical processes occurring during video pulsing of PIN diodes occur during rf excitation as well. Information obtained from comparing calculated and measured dc transients has been directly helpful in understanding rf limiter behavior.

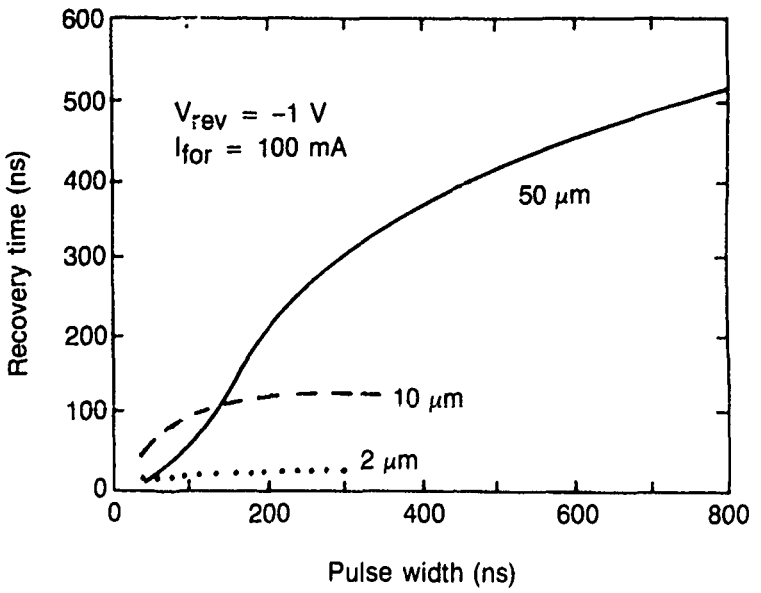


Figure 11. Measured recovery time versus forward-current pulse width for constant current amplitude and reverse bias voltage.

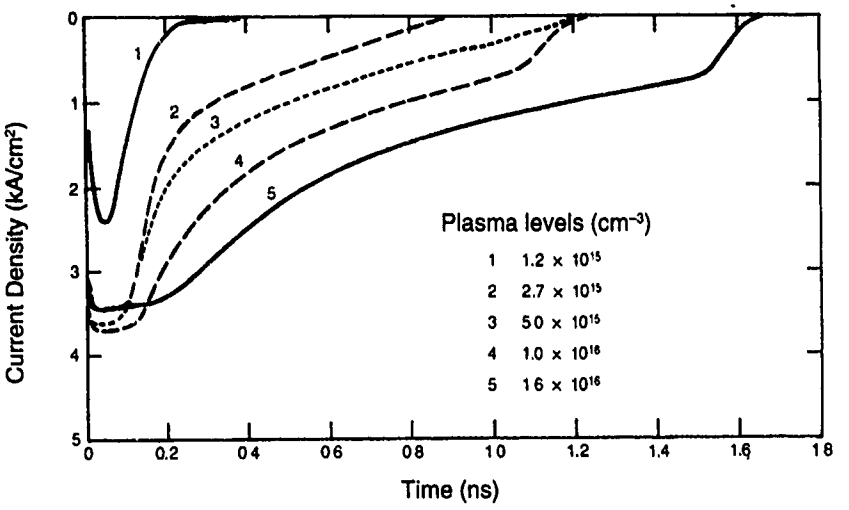


Figure 12. Current decay upon reverse switching of a 10-μm PIN diode. Applied voltage is 50 V. Parameter is plasma level of initial stored charge distribution.

5. Forward-Biased RF Conductivity

The rf impedance of PIN diodes under forward dc bias has been measured and calculated. There are several advantages for this mode, especially for the computations. The computer calculations are facilitated, since the half-cycle step calculations required for unbiased diodes are avoided. The measurement of the current and voltage waveforms is readily achieved. The forward biased turn-on is much faster than the unbiased turn-on. This reduces computer time, but more importantly, may be useful in preventing spike leakage with a delay-of-signal scheme [13]. The forward-biased rf conductivity is also dependent upon the recombination lifetime. This allows an alternate method of determining the lifetime from comparing measured and calculated data. Measurements of this type were first performed in the 1960's on thick PIN diodes at 10 MHz [14].

Forward current and voltage waveforms were measured with the use of a 6-GHz BW oscilloscope (Tektronix 7250). Typical forward voltage and current waveforms for a 10-μm PIN diode are shown in figure 13. The magnitude of the impedance was calculated from the current and voltage excursions and plotted in figure 14 as a function of time for three average current levels. The maximum estimated error in the process of determining the impedance is on the order of 20 percent. The measurements include the parasitic capacitance and inductance of both the diode pill-prong microwave package and the sample holder. The inductance of the diode package was measured with the use of a shorted diode package, as discussed in section 3.1. The capacitance of the probe and diode package was measured to be less than 1 pF, and the combined circuit and package inductance was estimated, with the use of a network analyzer, to be 3 nH.

The approximate dc voltage required in the calculations to produce the measured current levels indicated in figure 14 is obtained from figure 9. The superimposed 1-GHz rf voltage magnitude was varied to best fit the measured excursions. The calculated impedances are also shown in figure 14. The agreement is quite good. Note that the impedance drops as the current

increases, but not linearly in this high current range. It is impossible to calculate an impedance for the first cycle during turn-on, as may be seen by examining figure 13. An attempt to fit the calculated initial-cycle current and voltage waveforms to the measured waveforms has not been successful. One comparison of the waveforms is shown in figure 15. The measured current rises much more slowly than the calculated. This difference in current risetimes between measurements and calculations was also noted in the dc forward turn-on transients. In the dc measurements an extremely small approach current was sufficient to bring the measured turn-on time to agree with the calculations. This supports the supposition that inadequate initial and boundary conditions in the computer calculations are the major cause of the failure to obtain agreement. The initial filling of the unbiased PIN depletion region is a slow process limited by carrier diffusion and cannot be adequately simulated by the DIODE program.

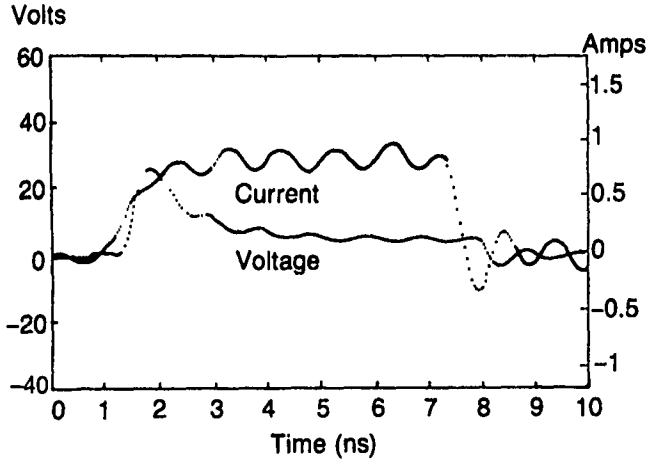


Figure 13. Typical oscilloscope traces of current and voltage response for a 10-μm PIN diode.

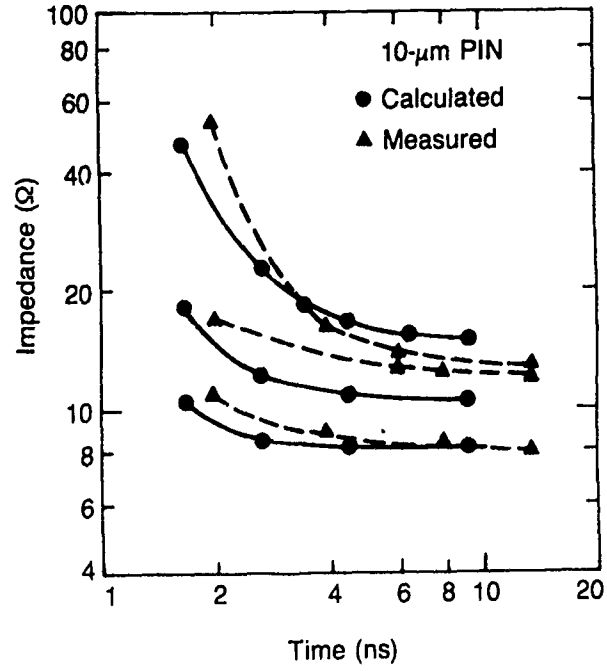


Figure 14. Measured and calculated rf impedance during forward turn-on for 10-μm diode at 1 GHz. Average current levels, from top to bottom, are 160, 330, and 710 mA for calculated data, and 150, 400, and 640 mA for measured data.

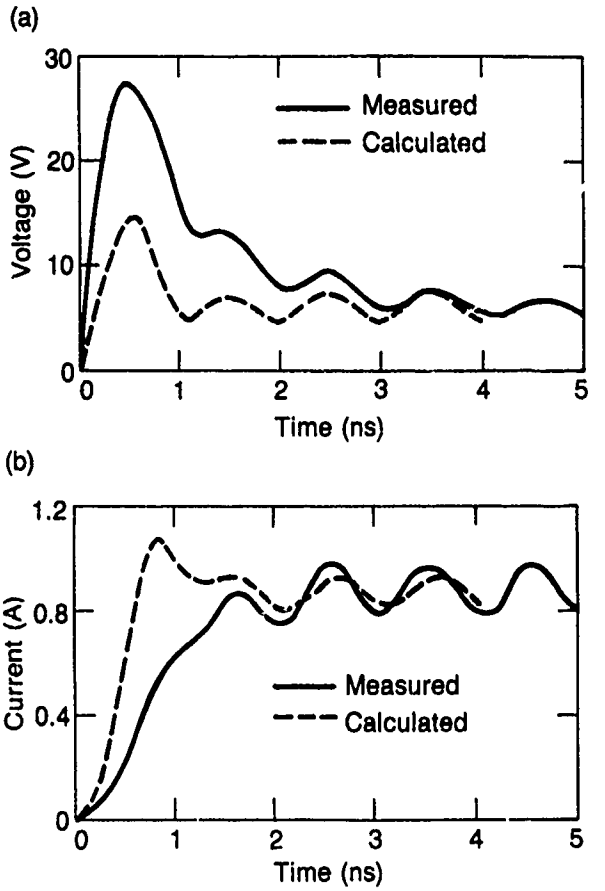


Figure 15. Comparison of measured and calculated forward turn-on transients of (a) voltage and (b) current for 10-μm diode. Frequency is 1 GHz. Calculated input voltage waveform had a peak-to-peak excursion of 12 V and an average of 48 V.

Measurements were also made on another 10-μm diode at lower frequencies. The variation of the measured quasi-equilibrium impedances with frequency is shown in figure 16. Also shown in the figure are the results of the computer calculations at the same frequencies. The impedance of the diode itself is nearly independent of frequency in this frequency range. With the addition of 2 nH for the diode package and sample holder inductance and 2 Ω for the current measuring resistance, the calculated impedance is in satisfactory agreement with the measured values, for a fixed current level (not the case in fig. 16). The calculations show that the total impedance varies linearly with frequency from 0.1 to 5 GHz. The fit to the experimental data was obtained with a recombination rate (inverse of the lifetime) of five times that of ideal intrinsic material. An increase in recombination rate increases the rf impedance, as shown in figure 17. The intrinsic material of most commercial diodes is not ideal, and many PIN diode limiters have gold doping to increase the recombination rate in order to reduce the recovery time.

The impedance during turn-on and turn-off transients may also be presented on a Smith chart. Figure 18 shows the forward turn-on and reverse recovery of a 10-μm diode at 5 GHz. The forward transient is seen to be inductive and the reverse recovery is capacitive. Also shown in the same figure are the results for a 50-μm PIN diode at 1 GHz. To build a very fast PIN limiter, consideration must be given to this impedance-versus-time profile. Note that the response of the 10-μm diode is about 10 times faster than the 50-μm diode in a 50-Ω circuit.

Figure 16. Measured and calculated quasi-equilibrium forward-biased rf impedances for 10-μm diode as a function of frequency. Average current levels are (A) 170, (B) 300, and (C) 400 mA.

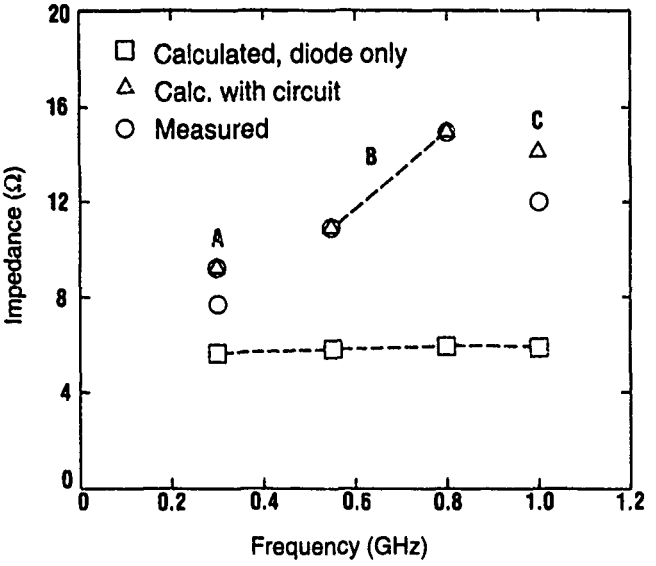


Figure 17. Calculated forward rf impedances as a function of recombination rate coefficient.

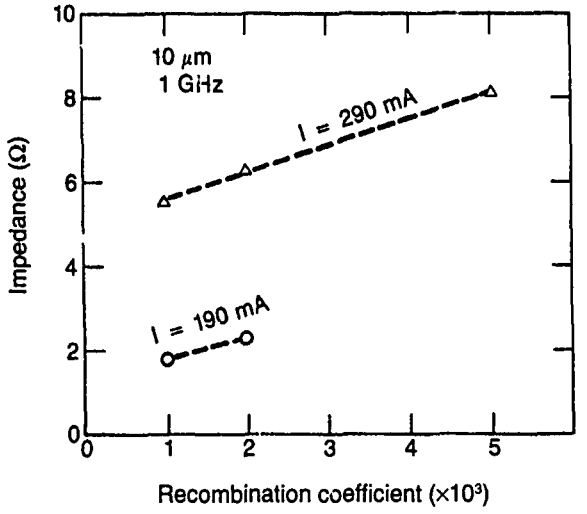
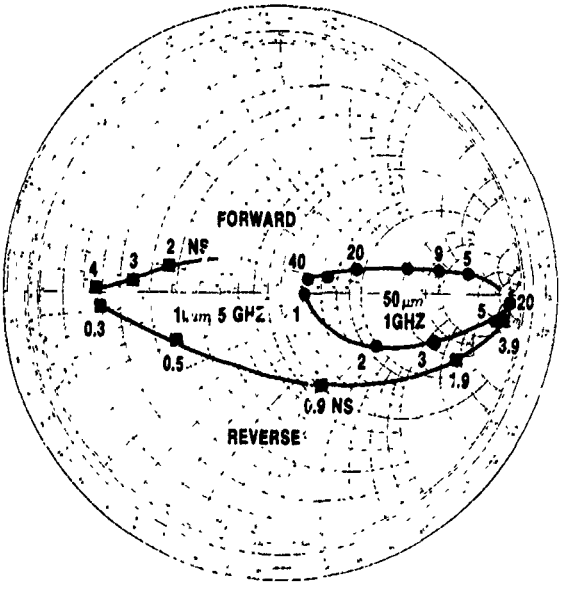


Figure 18. Transient impedances calculated for 10- and 50-μm diodes at 5 and 1 GHz, respectively. Times are given in nanoseconds.



6. Spike Leakage

It takes a finite time for any rf limiter, exposed to a fast-rising pulse, to produce its limiting action. This phenomenon has been designated spike leakage, from the high-power spike preceding in time the flat (in time) leakage. The spike in the gas plasma limiter is well understood to result from the time needed to achieve electrical breakdown. Avalanche breakdown is not the mechanism that initiates limiting in PIN diode limiters, and the physical mechanisms are, to some extent, controversial.

Spike leakage in a limiter is important since, if the energy in the spike is too great, the sensitive electronics being protected can be damaged or upset, even though the flat leakage level does not impose any danger. Generally, spike leakage energy increases with the width (thickness) of the intrinsic region of the PIN diode. Conversely, the danger of damage to the PIN diode limiter itself from excess absorbed power increases as the width of the intrinsic region decreases. This indicates that there is a trade-off between spike leakage and damage thresholds in selecting the width of the intrinsic region of PIN diode limiters. A better understanding of spike leakage is a requisite to designing improved limiters. Spike leakage may also be reduced by using dual diode limiters [15], where the second diode reduces the spike leakage from the first.

The forward turn-on switching transient was discussed in section 4. The same basic transit-time phenomena described in that section also apply for the rf turn-on transient. However, for the rf initiation, many cycles are required before equilibrium (flat leakage) is obtained. Experimentally, the time constant (rate of rise) of the applied rf signal is important. Spike leakage might not be observed with a microsecond risetime signal, but would be for a nanosecond risetime signal. For the calculations, as indicated in section 2, separate computer runs are required for each half-cycle of the rf input. One example of calculations with an increasing applied waveform is shown in figure 14 of HDL-TR-2124 [11] for a 1-μm PIN diode at 10 GHz. Two and one-half cycles were computed and avalanche breakdown was obtained.

6.1 Measurements

The measurement of the energy content of spike leakage requires certain choices in quantifying the power measured. Figure 19 shows the measured power passed by a 10-μm PIN limiter at several applied power levels. The risetime of the rf input is 1.5 ns. Figure 19(a) shows that a straight line extrapolation of the falling edge of the spike was used to determine the spike duration and energy. As the other figures show, the analysis is necessarily subjective. Nevertheless, it is quite evident that as the input pulse power is increased, the peak power of the spike leakage past the limiter increases while the duration decreases.

The measured energy in the spike leakage is shown in figure 20 for a 5- and a 1.5-μm diode. The energy in the spike increases about one decade for a

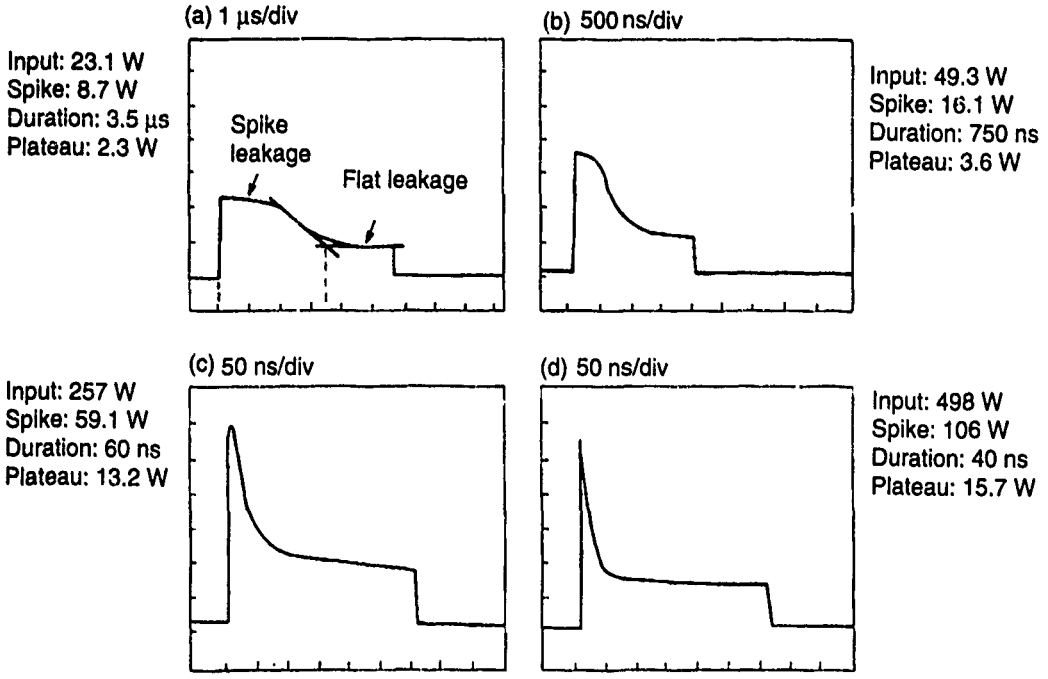
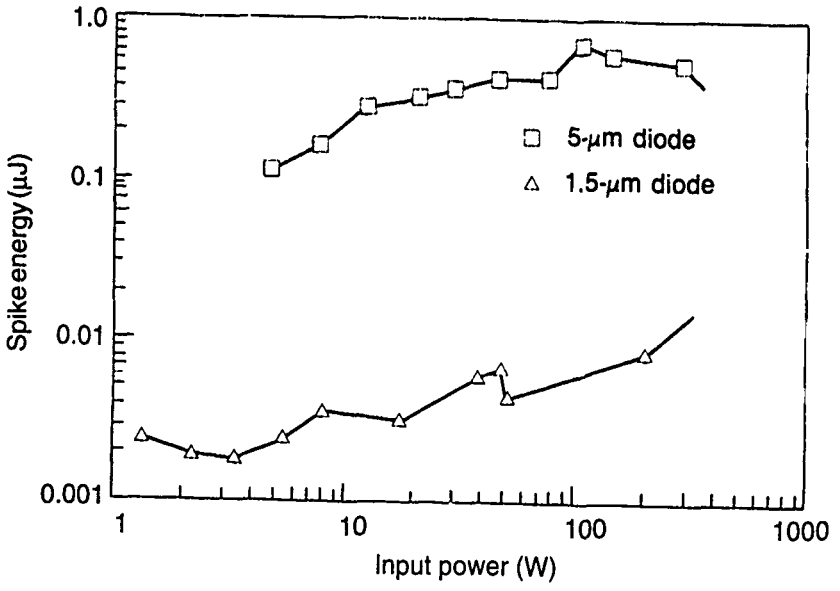


Figure 19. Spike leakage results of a 10-µm diode at four different input power levels at 8.79 GHz.

Figure 20. Spike energy as a function of input power for 1.5- and 5-µm I-region thickness diodes shows that energy in spike increases one decade for a three-decade increase in power.



three-decade increase of input power. The variation of spike energy with I-region thickness is much greater, as shown in figure 21. The measured spike leakage energy was also found to increase with frequency, as shown in figure 22. The risetime of the rf input pulse is 1.5 ns for the data in figures 19 through 22.

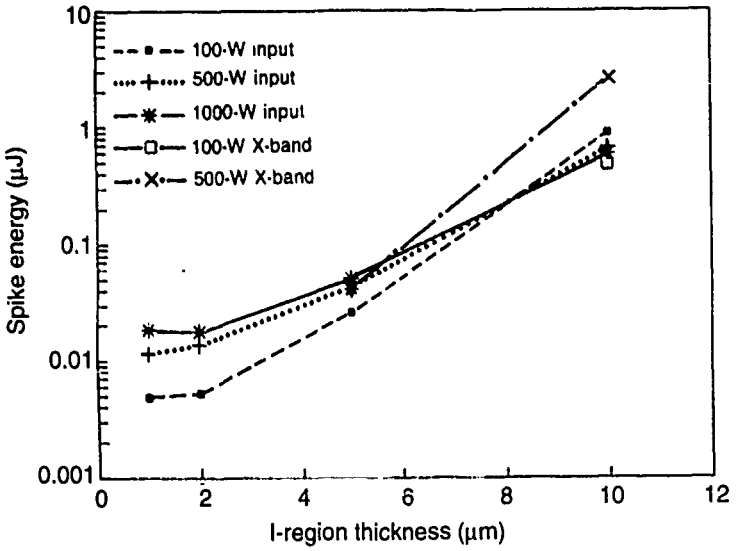


Figure 21. Spike energy increases as I-region thickness is increased. Data were taken at 1.5 GHz or at X-band with indicated input power.

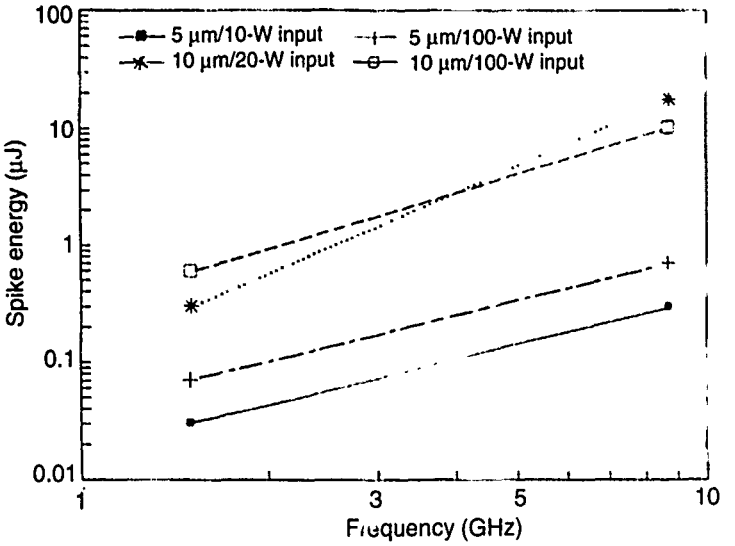


Figure 22. Measured spike leakage energy for 5- and 10-μm diodes as a function of frequency for several input powers.

6.2 Calculations

As discussed in section 2, the forward and reverse half-cycles of the rf input for a diode must be calculated in separate forward and reverse half-cycle runs. The forward half-cycle is similar to the initial portion of the video turn-on pulse and the reverse half-cycle is similar to the initial portion of the turn-off or recovery of the video pulse. Figure 23(a) shows the composite curve of the diode voltage as a function of time of the two half-cycles for a 10-μm PIN diode with a 400-V rf signal applied. The frequency is 1.5 GHz and the diode area is 3×10^{-4} cm^{-3}. The diode current is shown in figure 23(b). The voltage and current rectification is only moderate for this diode width and frequency. Rectification is discussed further in the next section.

The distribution of the carriers across the diode at selected times for the forward half-cycle of the oscillation of figure 23 is shown in figure 24. Evidence of the lower hole mobility as compared to the electron mobility is noted during the initial portion of the half cycle. The corresponding field

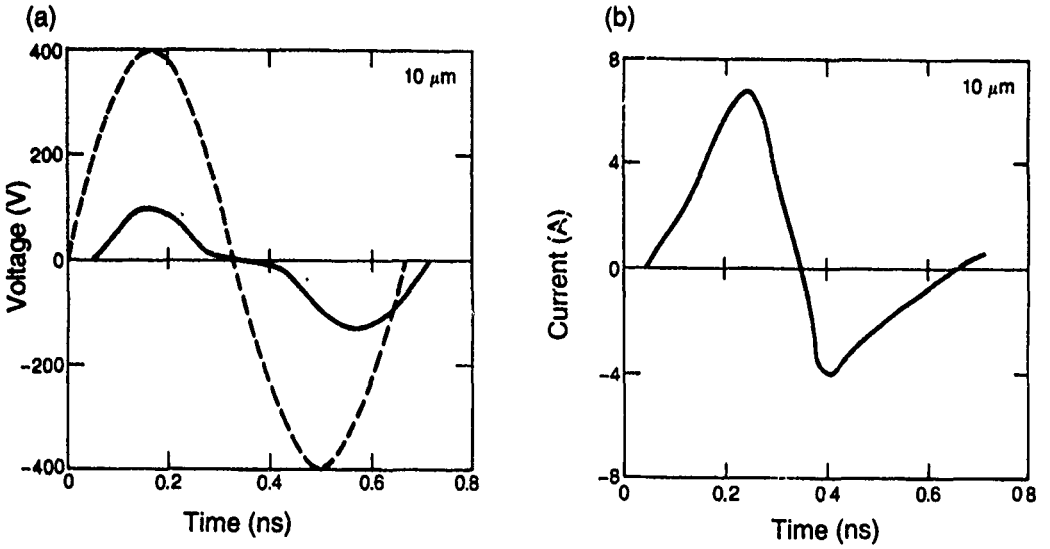


Figure 23. Composite of two half-cycles of 400-V applied, 1.5-GHz rf for 10-μm PIN diode: (a) dashed line is applied voltage and solid line is voltage across diode; (b) current is for a 3×10^{-5} cm^2 area diode.

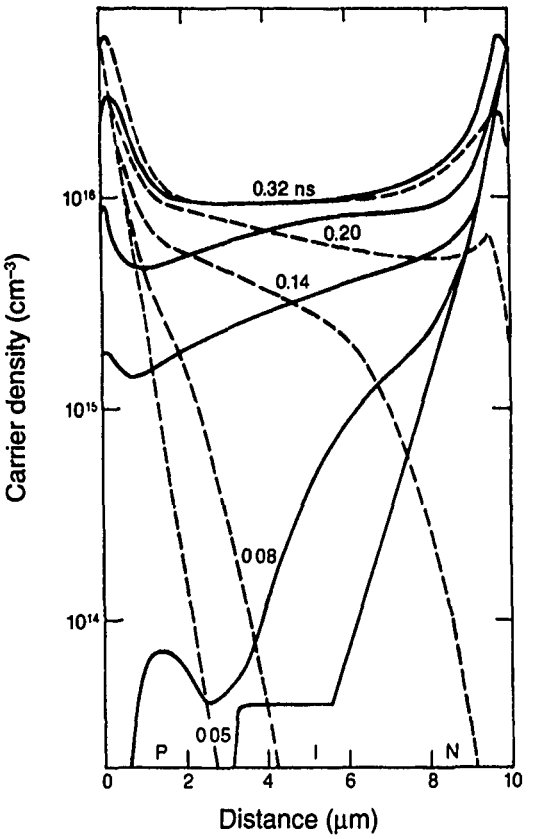


Figure 24. Distributions of electrons (solid lines) and holes (dashed lines) at selected times, in nanoseconds, for forward half-cycle of figure 23. Calculation was initiated with a space-charge-free distribution at 0.05 ns.

distributions for the carrier distributions of figure 24 are shown in figure 25. The fields are high in the central intrinsic region of the diode. The final distributions of figure 24 are used as initial conditions for the reverse bias half-cycle calculation. The reverse half-cycle carrier distributions and fields are shown in figures 26 and 27, respectively. Note that the electrons are removed from the diode much more rapidly than the holes, resulting in

Figure 25. Electric field distributions corresponding to charge distributions of figure 24.

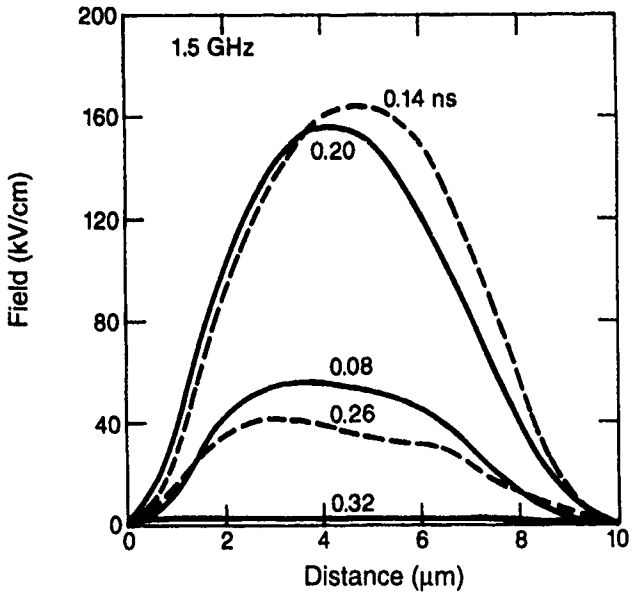
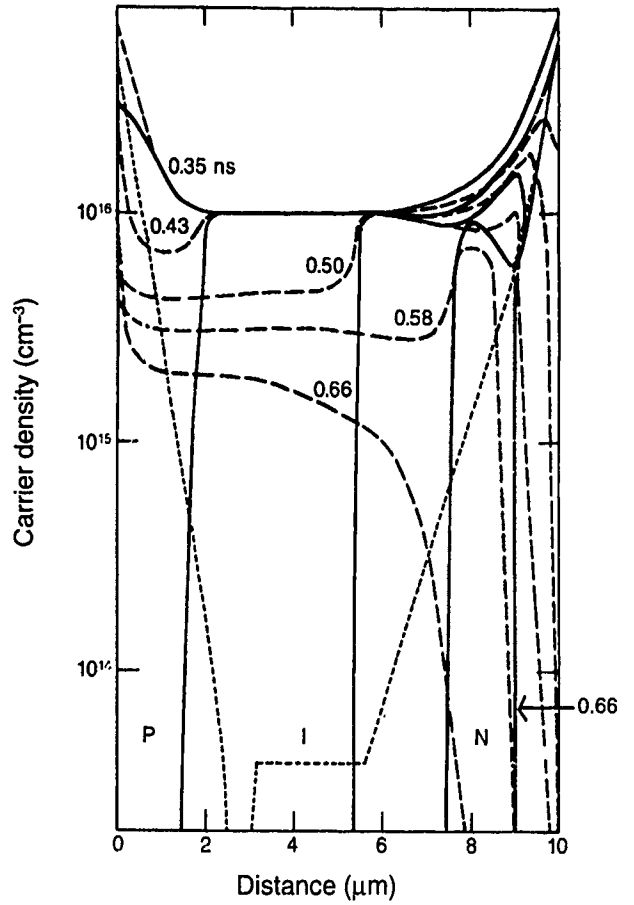
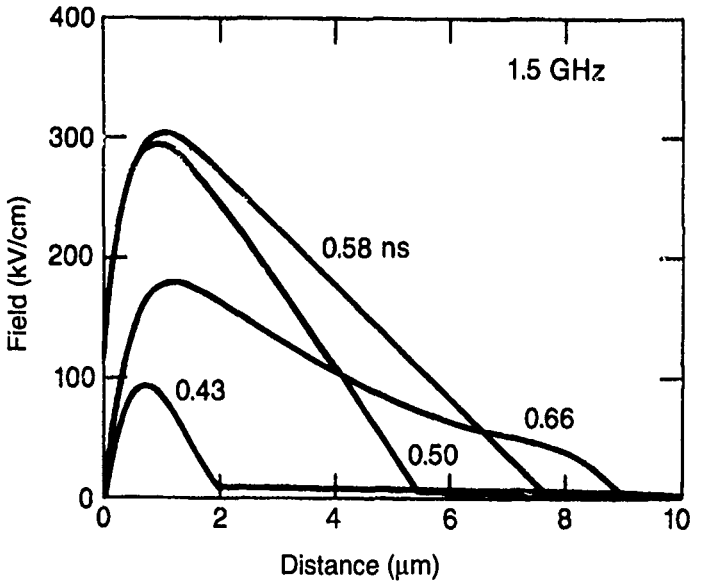


Figure 26. Distribution of electrons (solid lines) and holes (dashed lines) at selected times for reverse half-cycle of figure 23. Doping profile is given by short dashed lines.



higher fields on the P side of the diode. In figure 26, with reverse bias, the electrons move to the right and the holes to the left. The trailing edge of the electron distribution is extremely sharp because, as seen in figure 27, the field is higher at the trailing edge, and any backward diffusing electrons will move faster in the higher field and catch up. Further discussion is included in later sections.

Figure 27. Electric field distributions corresponding to charge distributions of figure 26.



It is impractical to try to calculate entire unbiased rf turn-on transitions, i.e., the full spike leakage transients of many tens or hundreds of cycles; the time and effort would be excessive. Instead, we have made calculations for only selected portions of the transient. These have been sufficient to increase our understanding of spike leakage. Figure 28 shows one example of the fit obtained between a calculated and measured turn-on transient for a 2-μm diode. The applied 1.5-GHz power reached its maximum of 100 W in about five cycles. As seen in figure 28, the second cycle was fit adequately with a calculated sinusoidal of 25 V; and the third cycle, with 55 V. The calculated stored charge remaining at the end of the reverse portion of cycle 3 was inadequate to measurably increase the amount of stored charge in the following forward half-cycle. Two reasons for undercalculating the stored charge, boundary conditions and unrealistic recombination rates, were mentioned previously. The stored charge had to be arbitrarily increased nearly an order of magnitude in order to fit the fifth reverse half-cycle. The result is also shown in figure 28.

The spike-leakage transient measurement of figure 28 was repeated with a second diode of the same lot. This time the applied (input) voltage signal was also recorded and is included in figure 29 for a 10-W input pulse. Although the measured input power was 10 W, the maximum voltage excursion was measured to be only about 23 V. This corresponds to a power of slightly under 5 W. The oscilloscope calibration was checked and found to be about 13 percent below the true voltage. The reason for the remaining error has not been ascertained. A comparison of figures 28 and 29 shows that there is a wide variation of the amplitude and shape of the forward half-cycles in figure 28 but very small variation in those of figure 29. Calculations show little variation in the forward half-cycle voltage waveforms. The variation shown in figure 28 may be caused by parasitics.

The increase in spike leakage power with increased input power is readily calculated for the various diode widths. However, the spike duration may

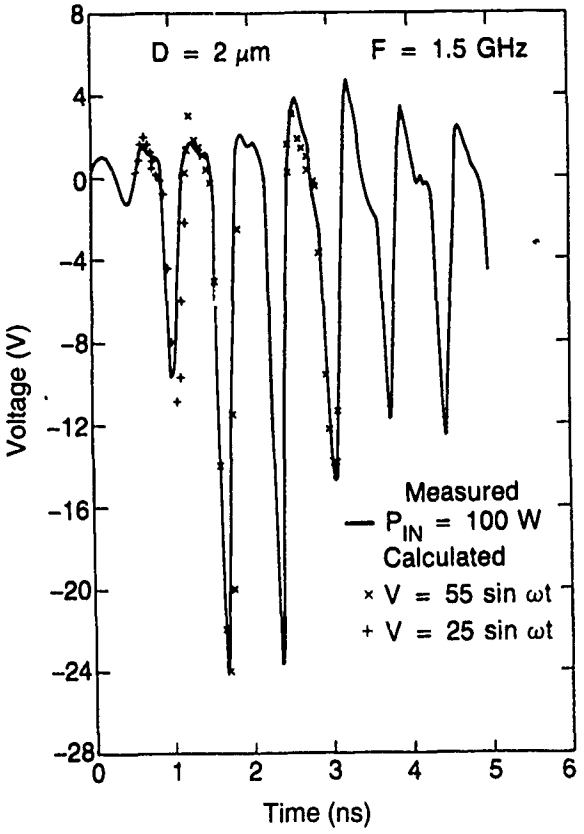


Figure 28. Comparison of calculated and measured turn-on voltage transient.

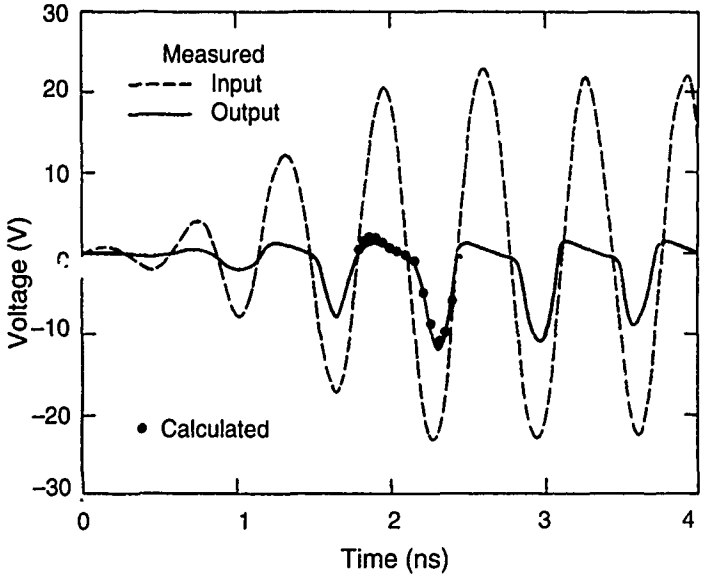


Figure 29. Measured input and output voltage transients for 2-μm diode. Input is 4.8 W at 1.5 GHz. Also plotted is one cycle calculated with 25 V maximum (each polarity) voltage input.

only be qualitatively seen to decrease with the increase in input power. This decrease in spike duration has been shown to result from the effect of increased stored charge in the forward half-cycle and the resulting longer time required to remove that charge during the reverse half-cycle. Space charge effects are dominant in slowing charge removal. This effect is also observed in dc reverse switching and other charge collection calculations [14].

It was shown in figure 24 that the lower mobility of the holes results in a slower transit time across the intrinsic region than that for the electrons. The field in the intrinsic region remains high until the holes complete their transit and form a plasma with low space charge fields. Most PIN diodes are actually P-ν-N diodes, with ν indicating low density of donors (excess electrons) of about $10^{14}\,cm^{-3}$ or less. It was decided to make calculations for a P-π-N diode, where π indicates a low density of acceptors (excess holes). Calculations with $\pi = 1 \times 10^{14}\,cm^{-3}$ did show a marginally faster forward turn on and a lower maximum voltage. Increasing π to $1 \times 10^{15}\,cm^{-3}$ resulted in a marked improvement, as shown in the inset of figure 30. Unexpectedly, the P-π-N diode showed a lower quasi-equilibrium impedance than the P-ν-N diode at low currents, as shown in figure 30. Experimental verification of this improvement will be required.

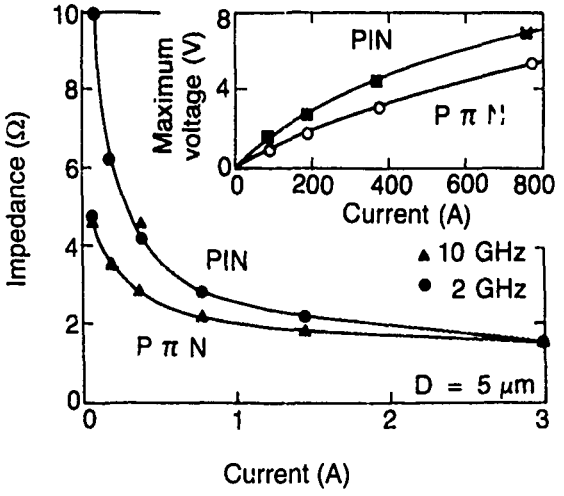


Figure 30. Comparison of quasi-equilibrium forward-biased impedances of 5-μm PIN and P-π-N diodes; π doping is 1×10^{15} cm^{-3}. Inset compares maximum turn-on voltage of two diodes.

6.3 Spike Leakage Paradigm

As a result of many calculations, the following paradigm has been proposed. At low powers, all the stored charges from the forward half-cycle are collected in the reverse half-cycle. At moderate input powers, a few stored (low mobility) holes remain at the end of the reverse half-cycle. These stored holes, in turn, reduce the turn-on time, as shown in section 6.2, and thus increase the charge stored in the next forward half-cycle. This process takes a large number of cycles before electrons also remain at the end of the reverse half-cycle. At this stage the effective diode width is reduced and the diode impedance rapidly drops. This can explain the long duration but rather sudden end of the spike leakage transient at moderate input power. At high input power, space charge effects are large enough to cause electrons to remain at the end of the reverse half-cycle and the transition is rapid.

This paradigm is also a plausible explanation for a cw hysteresis effect first observed by Deppe [17]. He observed that as the cw rf power was increased, the limiter output voltage increased nearly linearly with the input voltage until a sudden drop occurred. Further increase of the input power showed only a slight increase in limiter output voltage. Even this drop is not included

in the conventional limiter action. Moreover, once the limiter was turned on, the input power could be dropped below the transition point and the limiter output would remain low until it met the original curve. One hysteresis curve is shown in the next section (fig. 43, p 38) for a 10-μm diode. Once the cw input power exceeds the transition level near 20 W, the lower input-output power curve may be traversed in either direction. But once the input power is reduced to the level corresponding to the upper curve ("stored-charge level"), only that curve is followed until the input power once again exceeds the transition level. It is postulated that the transition level for cw is the point where stored charges remain at the end of the reverse half-cycle. Once this stage of redistributed charges and electric field is reached, the stored charges would remain even as the input power is reduced. The cw transition power is close to the pulsed power where limiter action is first observed. No cw hysteresis is observed for thin intrinsic region diodes (below 2 μm), and spike leakage is also quite small. There are no hysteresis effects under pulsed conditions, but the maximum power in the spike is nearly continuous with the upper cw leg, and the flat leakage is approximately the same as the cw lower leg above the transition.

7. Isolation

The flat leakage power is that constant power level which follows the spike leakage and which is transmitted past the limiter to the load or device to be protected. Ideally, the flat leakage remains nearly constant as the input power to the limiter is increased, up to a maximum isolation. The isolation, usually given in decibels, is the ratio of the output power to the input power. Thus, in the plateau region the isolation will increase nearly linearly with the input power. At some input power, the output power will rise nearly linearly again with the input power, defining a maximum isolation. Maximum isolation is generally somewhere between 10 and 40 dB. In practice, the plateau region is not flat, nor its boundary region sharp. Experiments guided by circuit analysis may be used to introduce capacitors or other elements to improve the shape of the plateau at a desired frequency.

7.1. Computation Methodology

The problems in computing spike leakage, discussed in section 6, are even more serious in isolation computations. One of the problems is correlating the input voltage waveform in the circuit of figure 3 with the experimental input rf power. This problem arises because we are using a lumped-element circuit to describe scattered waves on a transmission line shunted by a time-dependent element (the limiter). If the diode resistance were constant, the problem would be almost trivial. Omitting the reactive elements, the circuit of figure 3 is shown in figure 31, where the series and load resistors are 50 Ω, corresponding to the experimental circuit. The voltage source sees an effective resistance of

$$R_{eff} = 50 + \frac{50R_D}{50 + R_D}, \tag{4}$$

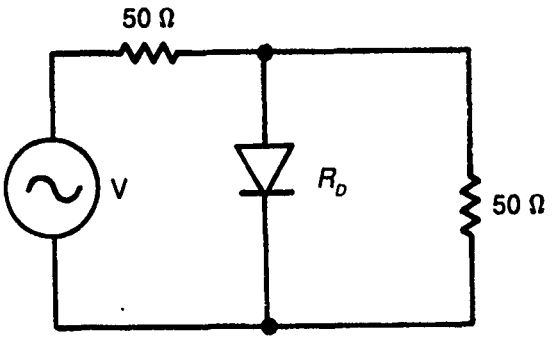


Figure 31. Basic circuit used to compute input rf power as a function of input voltage.

where the diode resistance is R_D. As R_D varies from ∞ (no current flow) to 0 in the limit, R_{eff} varies from 100 to 50 Ω. The input rf power is given by

$$P_{in} = V^2/2R_{eff} \ , \tag{5}$$

where the factor 2 is required since V is the peak voltage excursion, and the waveform is assumed sinusoidal.

The problem is that the diode resistance, R_D, is unknown before the calculations and therefore the effective input power is also unknown. When the calculations are completed, R_D may be estimated by several methods. The one used most often in our evaluations is to graphically integrate the diode power, P_D, the product of the instantaneous current and voltage, during one full rf cycle. The power through the 50-Ω load (P_L) was also similarly obtained. The diode resistance is then given by

$$R_D = 50\ P_L/P_D \tag{6}$$

since the voltage is the same for the diode and load.

In theory, the diode resistance could be obtained by integrating the instantaneous ratio of the diode voltage and current. In practice, large errors arise from this method due to calculation instability at low currents and in other conditions. Obtaining average currents and voltage during the full cycle has been found more practical. Some comparisons of results obtained from the various methods of calculating R_D will be given later.

For convenience in obtaining the input power corresponding to the applied voltage amplitude, a graph has been prepared (see fig. 32). The input power given by equation (5) is used to define a parameter N defined by

$$P_{in} = V^2/100N \ . \tag{7}$$

Comparison of equations (5) and (7) shows $N = R_{eff}/50$. N has been calculated for $1 \le R_D \le 1000\ \Omega$ and is plotted in figure 32. Also shown in the same figure is N plotted as a function of P_D/P_L. The maximum error in P_{in} from the maximum variation of N (from 1 to 2) is a factor of 2, or 3 dB. Since considerable effort is needed to obtain N, and other errors are of this order of magnitude, not all of the following data have used equation (7). In most cases, N is approximately 1.5.

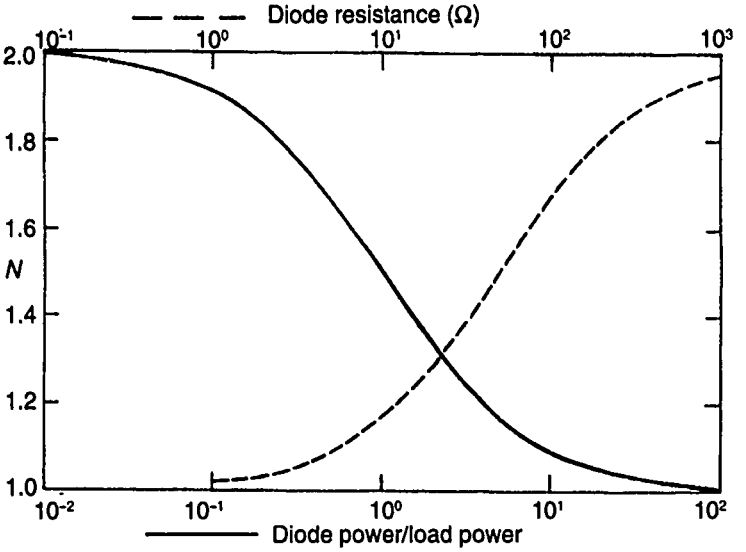


Figure 32. Graphical determination of N to be used in equation (7) to obtain input power.

7.2 Calculation Results for 5-μm Diode

The instantaneous power into the diode $P_D(t)$, the product of the diode current and voltage, is integrated as a function of time for the forward and reverse half-cycles individually. The sum of the forward and reverse integrated power divided by the rf period gives $P_D(av)$. The power to the load is given by integrating $V^2(t)/50$ in the same manner. Figure 32 is then used to obtain N, and equation (7), to obtain P_{in}.

An example of the procedure for a 5-μm PIN diode at 1.5 GHz follows. For a 50-V-amplitude applied signal, the calculated diode and load power as a function of time are shown in figure 33. The forward average diode power is 1.88 W and the reverse is 0.38 W, yielding a full-cycle average P_D of 1.13 W. The forward average load power is 0.25 W and the reverse is 5.8 W, for a full-cycle average of 3.03 W. The ratio of P_D to P_L is 0.37. From figure 33, N is found to be 1.73 and R = 135 Ω. From equation (7) P_{in} is determined to be 14.5 W. Thus for the 50-V amplitude calculation, the input power is 14.5 W, and the diode dissipates 1.13 W and transmits 3.03 W to the load. This indicates that 10.3 W is reflected back to the source.

The power to the load as a function of input power is plotted in figure 34 for peak voltage amplitudes from 10 to 1000 V. The experimental measurements of both the spike and flat leakage for a 5-μm PIN diode at 1.5 GHz are also shown in the same figure. The measured threshold of limiter action is about 0.1 W and the maximum isolation varies between about 10 and 13 dB.

The calculated dissipated power is intermediate between the measured spike and flat leakage curves. This is attributed to the use of the stored charge after the first forward half-cycle for the reverse half-cycle. For a 5-μm PIN, many cycles are required for the stored charge to reach equilibrium, as discussed in section 6.

The stored electron charge at the end of the 50-V forward half-cycle calculation discussed above is shown in figure 35. The doping profile is included in

Figure 33. (a) Power dissipated in a 5-μm diode during one cycle at a frequency of 1.5 GHz and (b) power transmitted to a 50-Ω load (output power) for same cycle.

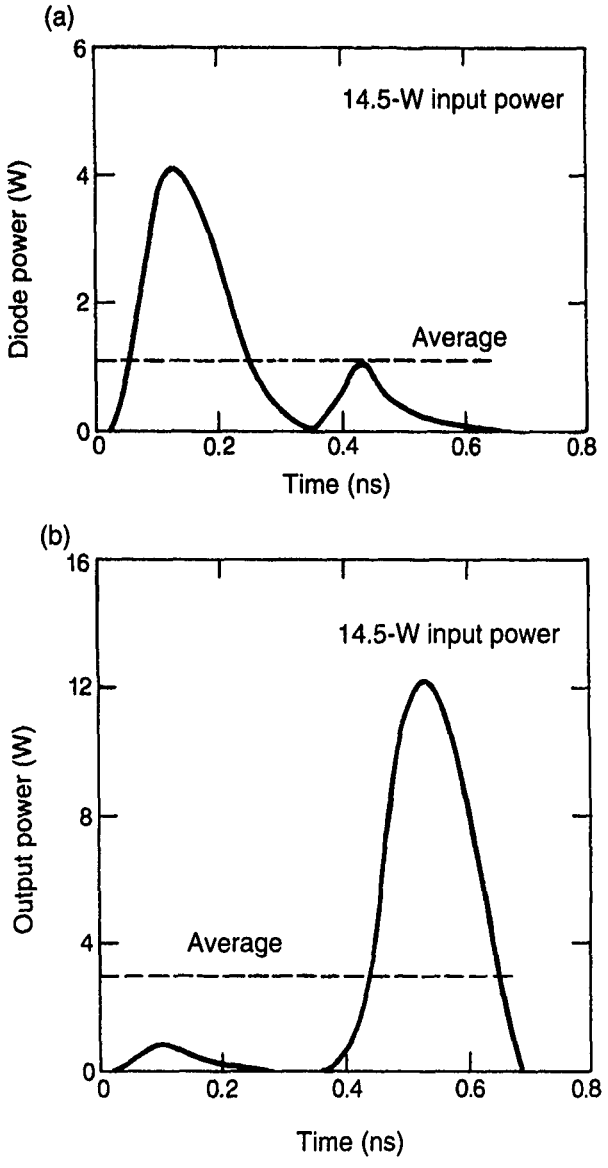
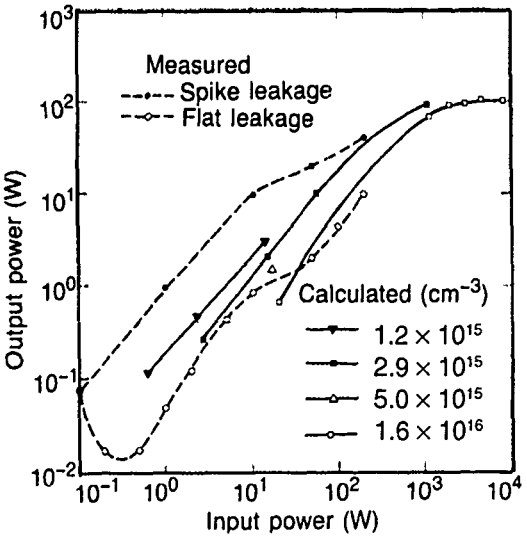


Figure 34. Measured and calculated output power (flat leakage) as a function of input power for a 5-μm diode at 1.5 GHz. Measured spike leakage power is also plotted. Reverse half-cycle calculations used varying plasma densities, as listed.



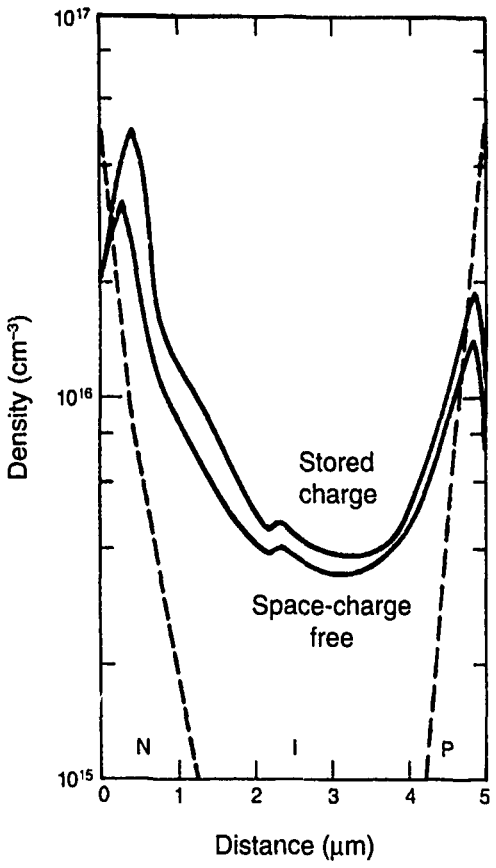


Figure 35. Stored electron charge at end of forward half-cycle for 14.5-W applied power with and without initial stored charge.

the figure. The hole and electron densities are equal, and the electric field is a maximum, just about at the position where each reaches a local minimum. This equal density value, the plasma density, is chosen to designate the charge density for the stored charge. The thus defined stored charge is plotted as a function of the forward voltage in figure 36 for the 5-μm diode. These curves are for field-free initial conditions; if stored charges remain at the end of the reverse half-cycle, the new forward calculations would give a larger stored charge.

Further calculations were made with various values of stored charges for the reverse half-cycle. The voltage peak was 50 V and the input power was calculated to be from about 15 to 20 W. The resulting waveforms are shown in figure 37 and the power through the load is shown in figure 34. The actual distributions used were from a library of similar distributions but not from this series of calculations. Small changes in the stored charge distributions have been found to have a negligible effect on the resulting waveforms. The stored charge densities (as defined above) used in the calculations were 1.2×10^{15}, 2.9×10^{15}, 5.0×10^{15}, and 1.6×10^{16} cm^{-3}, and by interpolation of the curve of figure 36, these correspond to forward voltages of approximately 14, 40, 80, and 400 V, respectively. As seen in figure 34, the largest stored charge distribution gave a P_L value, in agreement with the experimentally measured value. Also shown in figure 35 is the forward half-cycle calculated with the stored charges remaining after the reverse cycle which was calculated with

Figure 36. Stored charge at end of forward half-cycle as a function of maximum voltage applied at 1.5 GHz. Parameter is thickness of intrinsic region of diode.

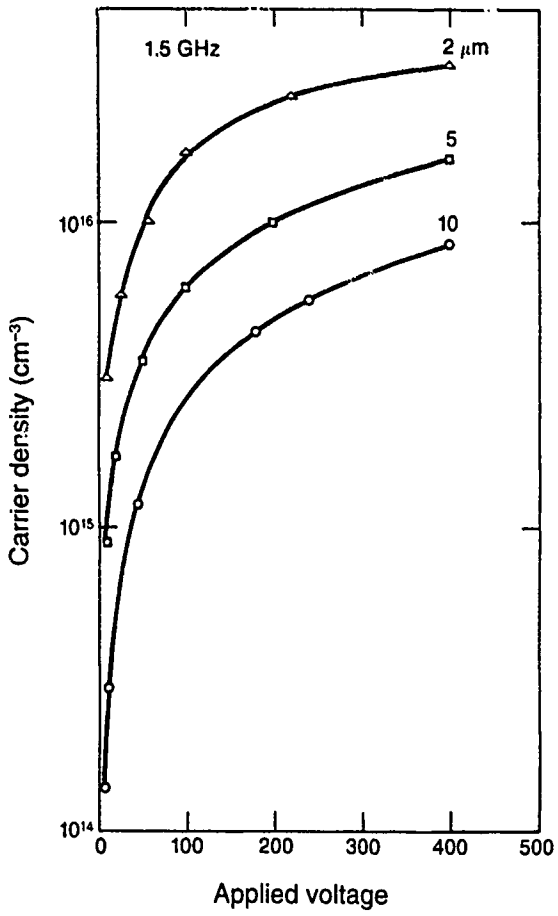
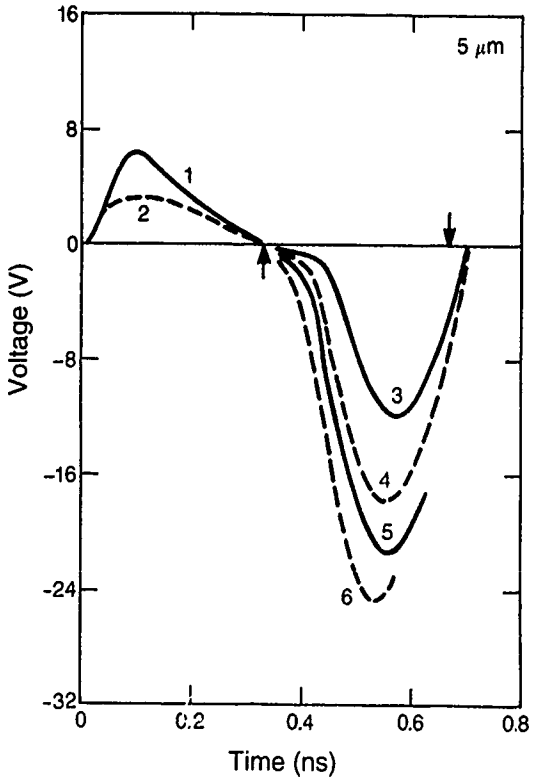


Figure 37. Voltage waveforms calculated with various initial conditions. For forward half-cycle, 1 is for no stored charge and 2 is with 1.6×10^{16} stored charge at the end of reverse half-cycle. For reverse half-cycles stored charge levels are (3) 1.6×10^{16}, (4) 5.0×10^{15}, (5) 2.9×10^{15}, and (6) 1.2×10^{15} cm^{-3}.



the largest initial stored charge. The stored charge at the end of the enhanced forward-cycle was $4 \times 10^{15} cm^{-3}$, as compared to $3.5 \times 10^{15} cm^{-3}$ calculated with no initial stored charge. This small increase indicates that other limitations of the calculations probably are more important in the attempt to fit the measured data. As indicated previously, these are believed to be the high recombination rates and the low maximum doping levels at the boundaries. The effect of the recombination rate is discussed later.

The leveling off of P_t for an input power of above 1-kW input power shown in figure 34 is due to avalanching occurring during the reverse half-cycle. Avalanching increases the diode current and thus reduces its impedance. Although the dc reverse breakdown of a 5-μm PIN is only 122 V, approximately 300 V must be applied for a 1.5-GHz rf pulse to initiate appreciable avalanching. This results from the formative time lag, the time for the avalanche to build up. The current and voltage pulses during the reverse half-cycle for the 5-μm PIN diode with a 400-V, 1.5-GHz rf are shown in figure 38. The initial current peak is due to the collection of the stored charges. When the voltage exceeds about 130 V, rapid avalanching occurs, and the current through the 50-Ω series resistance drops the voltage across

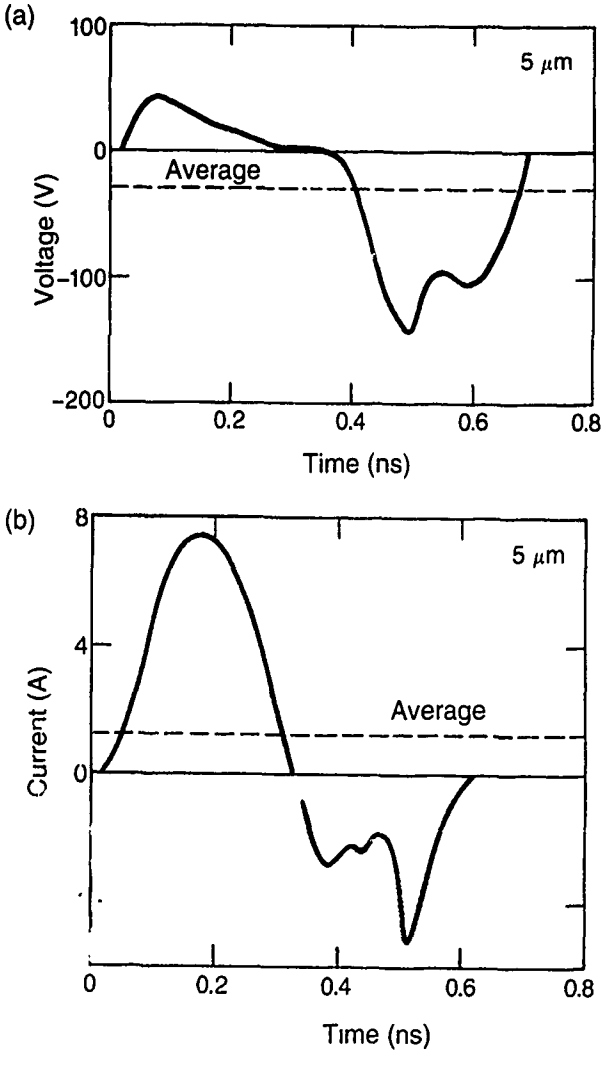


Figure 38. Calculated (a) voltage and (b) current for one cycle of 1.5 GHz with a peak applied voltage of 400 V. Avalanching begins at 0.5 ns during reverse half-cycle.

the diode. Higher stored charges lower the avalanche voltage [7]. The instantaneous diode forward and reverse half-cycle resistances are plotted in figure 39. With the omission of the uncalculated high resistance portions of each half cycle, the average resistance for each was determined. The results are included in table 1. Also shown in table 1 are the forward, reverse, and average resistances calculated using equation (6). The agreement between the two methods is satisfactory. The effect of avalanching on diode dissipation is discussed in section 8.

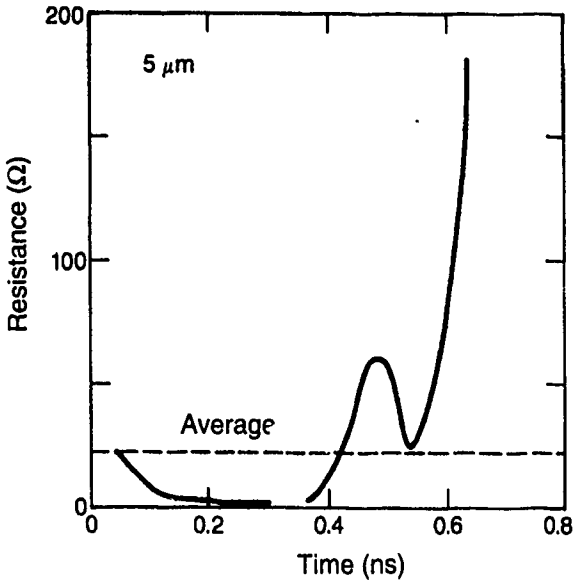


Figure 39. Calculated resistance from voltage and current curves of figure 38.

Table 1. Comparison of calculated resistances

A. From current and voltage transients

Averaging interval	I_{av} (A)	V_{av} (V)	R_{av} (Ω)
Forward half cycle	4.34	18.2	4.2
Reverse half cycle	1.88	77	41
Full cycle average	3.11	47.6	15.3
Full cycle average of R_{av}			22.6

B. From the ratio of P_D to P_L

Averaging interval	P_D (W)	P_L (W)	Ratio P_D/P_L	R_D (Ω)
Forward half cycle	89.7	10.6	8.5	6.5
Reverse half cycle	160	146	1.1	46
Full cycle average	125	78.5	1.6	30
Full cycle average of R_D				26.3

Note: *I_{av} = average current, V_{av} = average voltage, $R_{av} = V_{av}/I_{av}$, P_D = power dissipated in the diode, P_L = power dissipated in the load resistor, and R_D = diode resistance computed from figure 32.*

7.3 Calculations for Other Diode Widths

Measurements of spike and flat leakage have been made for PIN diodes ranging in thickness from 1 to 50 μm. A composite plot of flat leakage measurements for input powers up to 200 W is shown in figure 40 for a frequency of 1.5 GHz. The results for the 1-μm diode show no spike leakage, and the initiation of limiting is gradual. All the wider diodes show a sudden threshold for limiting and all show approximately the same maximum isolation. Only the threshold for limiting is strongly dependent upon the diode thickness.

Measurements on one 2-μm PIN diode have been made only up to a maximum P_{in} of 2 W, but a second diode was subjected to a maximum of 200 W. The results are shown in figure 41, together with results from calculations for 1.5 GHz. Both the measured and calculated load power show slightly greater isolation than was observed for the 5-μm diode at the same low powers. At higher powers, avalanching occurs at a much lower voltage for the 2-μm diode, and P_{out} is calculated to level out at about 20 W as compared to 200 W for the 5-μm diode. The dc reverse breakdown is about 60 V. The power dissipated by the 2-μm diode is also shown in figure 41. The diode power increases sharply as the power to the load levels off. Measurements were also made on an improved (lower parasitic package, see sect. 3) 2-μm diode with the results shown in figure 42. The maximum isolation at 500 W is about 27 dB.

Fairly extensive calculations have also been made for a 10-μm diode at frequencies from 0.5 to 2.0 GHz. The comparison of the calculated and measured output power (P_L) as a function of P_{in} is shown in figure 43. The fit above the measured threshold is satisfactory. Also shown on the same graph are the measured cw hysteresis curves. The variation of the output power as a function of input power shows but a small frequency dependence, but the waveforms show considerable variation.

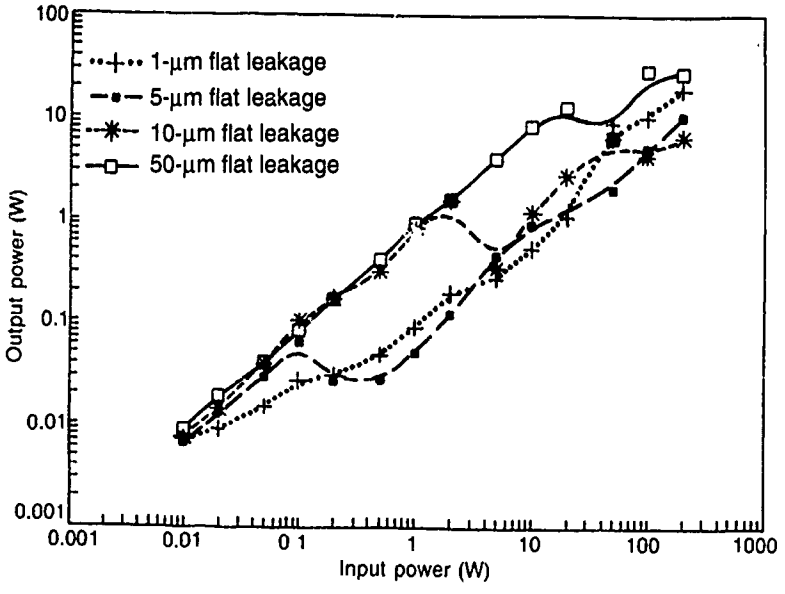


Figure 40. Measured flat leakage power as a function of input power for diode of various intrinsic region thicknesses.

Figure 41. Comparison of two measured and one calculated output-power curves as a function of input power at 1.5 GHz for 2-μm diodes. Also plotted is calculated power dissipated in diode.

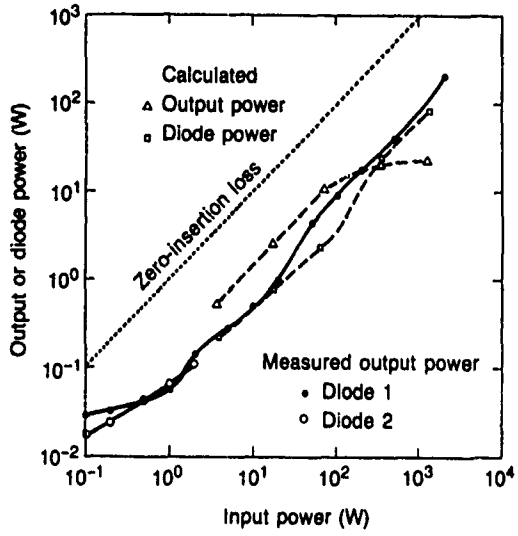


Figure 42. Measured output power as a function of input power for an improved 2-μm diode at 1.5 GHz.

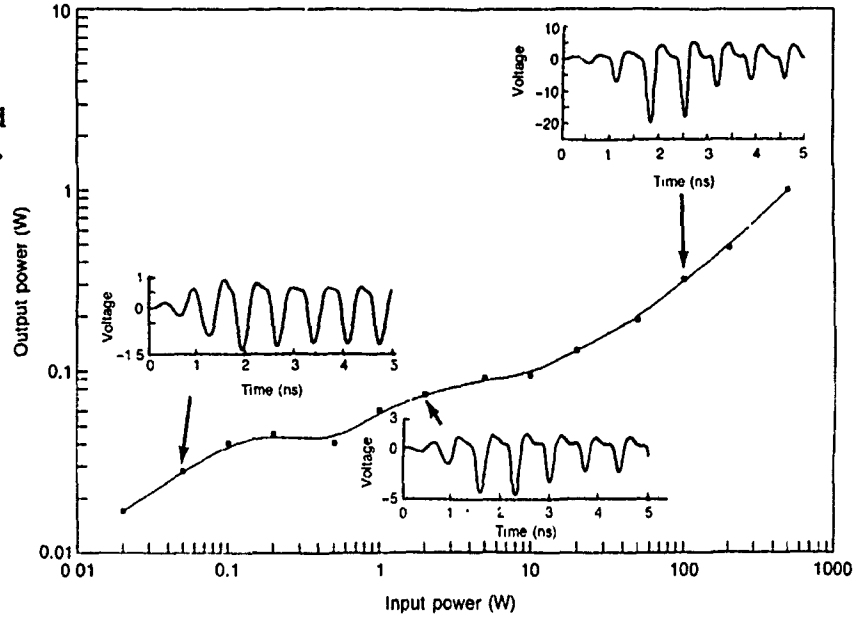
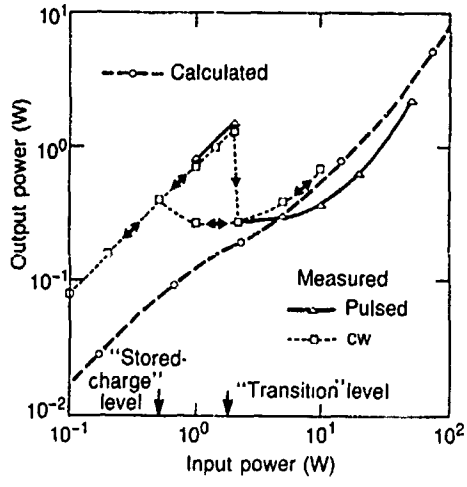


Figure 43. Comparison of measured short pulse (600 ns) and cw output power as a function of input power at 1.5 GHz for 10-μm diode. CW curves show a hysteresis effect. Also shown are corresponding calculated results.



One quantitative measure of the diode voltage waveform is the rectification ratio, V_{RR}, defined as

$$V_{RR} = 1 - \frac{V_F(max)}{V_R(max)} , \qquad (8)$$

where $V_F(max)$ is the maximum forward voltage and $V_R(max)$ is the maximum reverse voltage of the diode. Figure 44 shows the variation of V_{RR} with input power for the 2- and 10-μm diodes at selected frequencies from 0.5 to 5 GHz. In this frequency range the 2-μm diode is a better rectifier (V_{RR} is closer to 1) than the 10-μm diode. Each diode shows poorer rectification as the frequency increases. These calculations confirm the need for a dc return in a limiter circuit.

The average rectified current, I_{av}, may also be calculated from the difference between the average forward and the average reverse current. Figure 45 shows the variation of I_{av} as a function of input power for the 10-μm diode at selected frequencies. The large scatter at the highest frequency is believed due to our failure to adjust the stored charge as a function of frequency. Also shown are the corresponding measured values. For a direct comparison between the calculations and measurements, a large inductance should be used in the external circuit for the calculations to obtain a dc current. However, the time required to reach equilibrium makes this impractical. Considering the inadequacy of the circuit used in the calculations, the quantitative disagreement between the calculated and measured rectified current is not unexpected. Both the calculated and measured curves have a slope of near one-half.

Further information can be obtained by comparison of the calculated and measured voltage waveforms at various input powers. Figure 46 presents selected calculated voltage waveforms for a 10-μm diode at 0.5 GHz. The waveforms are insets in a plot of $P_{out} = P_L$ as a function of P_{in}. The initial small negative voltage maximum for the P_{in} = 40-W calculation is the result of the 0.5-nH inductance used in the calculations. At the higher power of P_{in} = 230 W, the inductance maximum has disappeared. Double voltage maxima in the

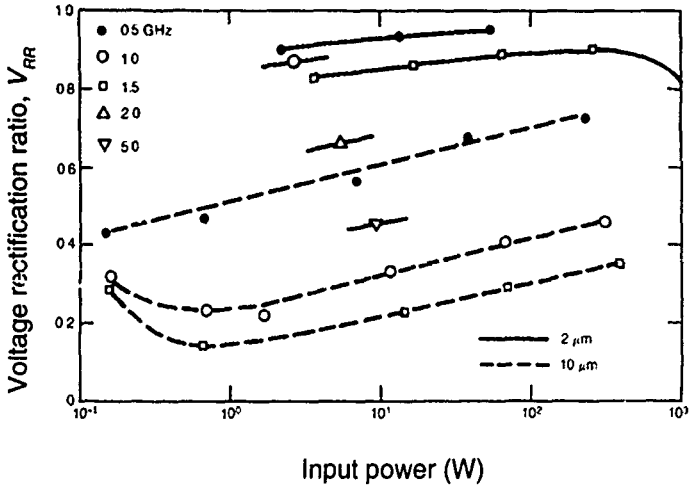


Figure 44. Voltage rectification ratio, as defined by equation (8), plotted as a function of input power for two diode widths. Parameter is applied frequency.

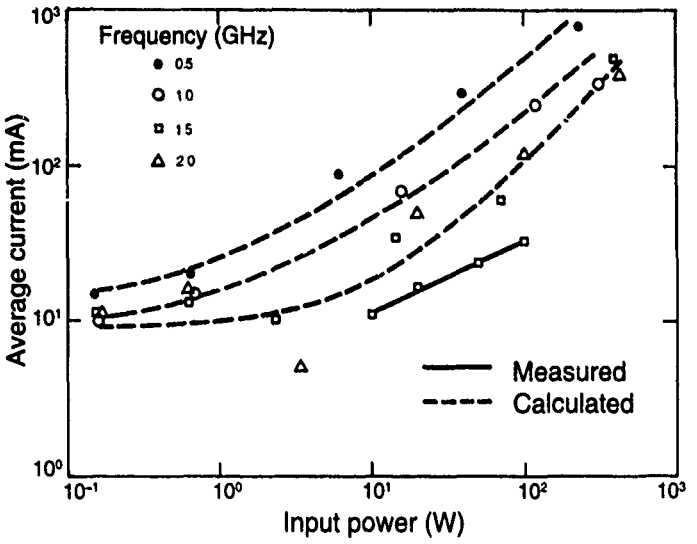


Figure 45. Average current over a full cycle calculated as a function of input power. Parameter is frequency. Also included are measurements at 1.5 GHz.

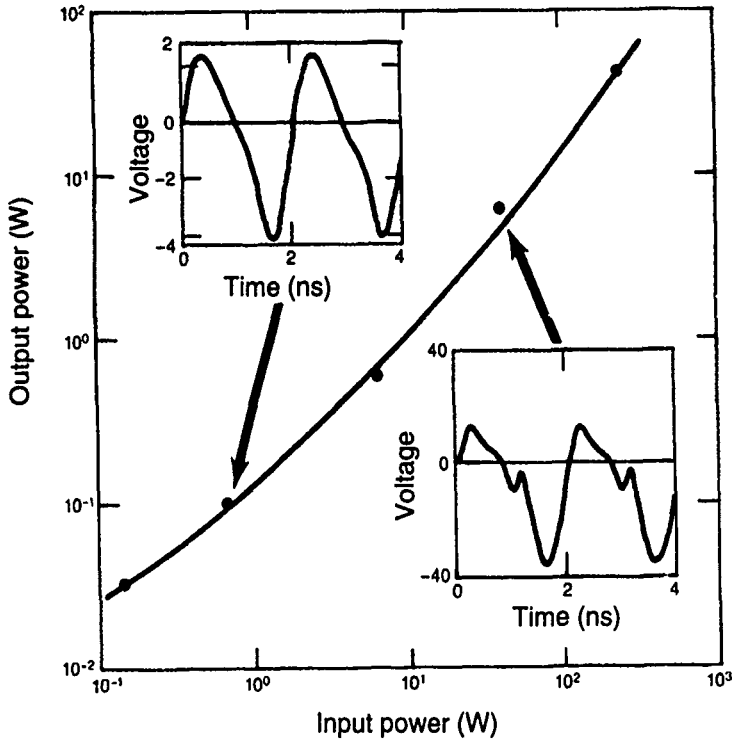


Figure 46. Calculated voltage waveforms are insets of a plot of output power as a function of input power for 10-μm diode at 0.5 GHz.

negative half-cycle were observed experimentally for the 2-μm diode, but not for the 10-μm diode. Experimentally, the double-voltage maximum was observed at intermediate powers, but not at lower or higher powers. Measured voltage waveforms are shown in figure 47 for a 10-μm diode at 0.45 GHz. At the lowest input powers, the measured voltage waveform is sinusoidal, whereas the calculated waveform is almost sawtooth. This again shows that no appreciable current flows in the measurements at these low powers. The highest power measured waveform has a shoulder whereas the calculated waveform has a local maximum. In this case a smaller inductance used in the calculations would give a better fit.

Calculated voltage waveforms for a 10-μm diode at 1.5 GHz are shown as insets in figure 48. The inductive voltage peak is essentially equal in magnitude to the (nearly) zero-current voltage peak for the P_{out} = 0.8-W calculations. Experimentally, the inductive peak has been observed to exceed the second peak in some cases. Again, at the higher powers the second peak increases more rapidly than the first (not illustrated). Measured voltage waveforms for a 10-μm diode at 1.5 GHz are shown as insets in figure 49. The low power waveform is visibly nonsinusoidal (dV/dt is greater in magnitude for the rising portion of the forward half-cycle than for the falling portion), even though P_{out} is almost equal to P_{in}. At the highest power the waveform has a flatter region just before the forward half-cycle. No explanation is available for this flattening.

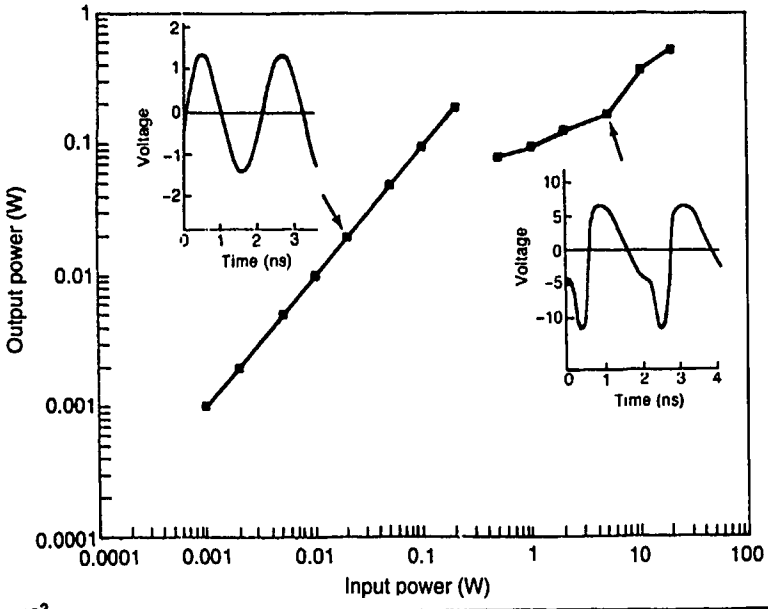


Figure 47. Measured voltage waveforms are insets of a plot of output power versus input power for 10-μm diode at 0.45 GHz.

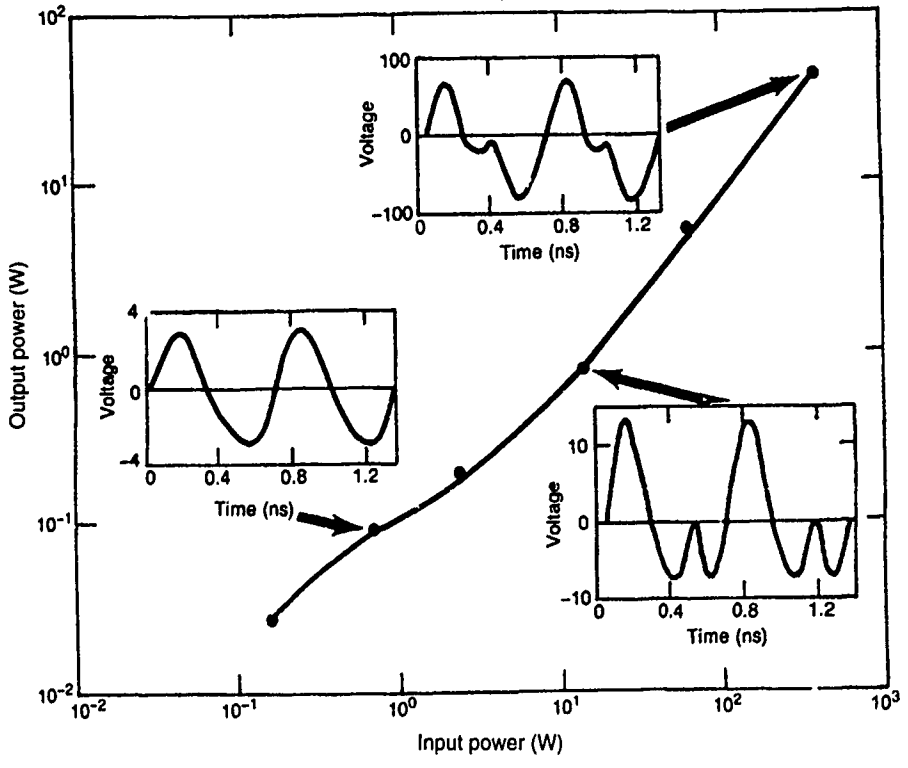


Figure 48. Calculated voltage waveforms for 10-μm diode at 1.5 GHz are insets of an isolation plot.

Figures 43 and 49 show isolation (output versus input) measurements for two different 10-μm diodes at 1.5 GHz. The two measurements are replotted in figure 50, together with the calculated curve. In the range from 5 to 100 W, the calculated curve is bracketed by the measured curves. Although the leveling of the output power at high power of the measured curve resembles the calculated effect of avalanching, the calculations show that much higher powers would be required to initiate avalanching. The flattening is probably associated with increasing reflected power, but is otherwise unexplained.

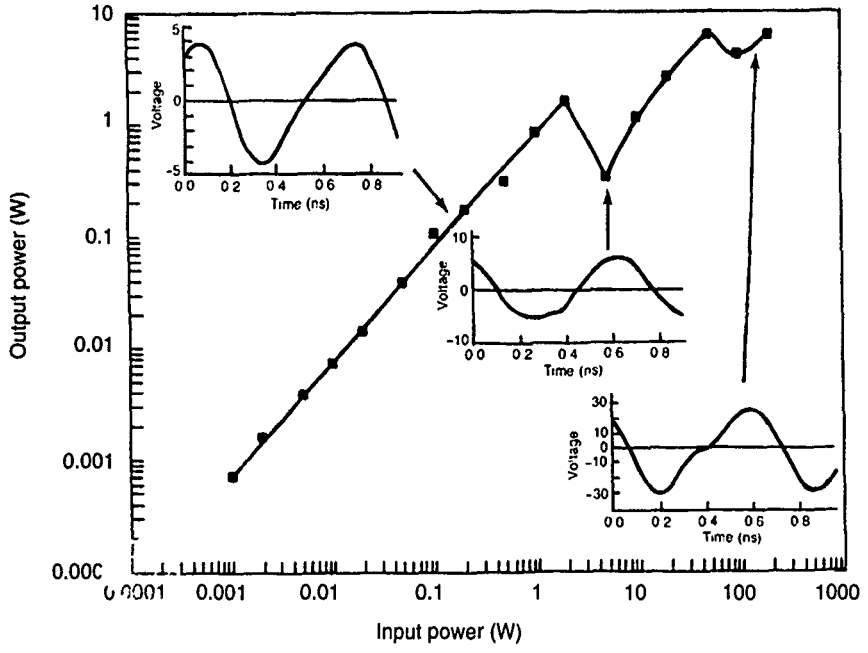


Figure 49. Measured voltage waveforms for 10-μm diode at 1.5 GHz as insets in an isolation plot.

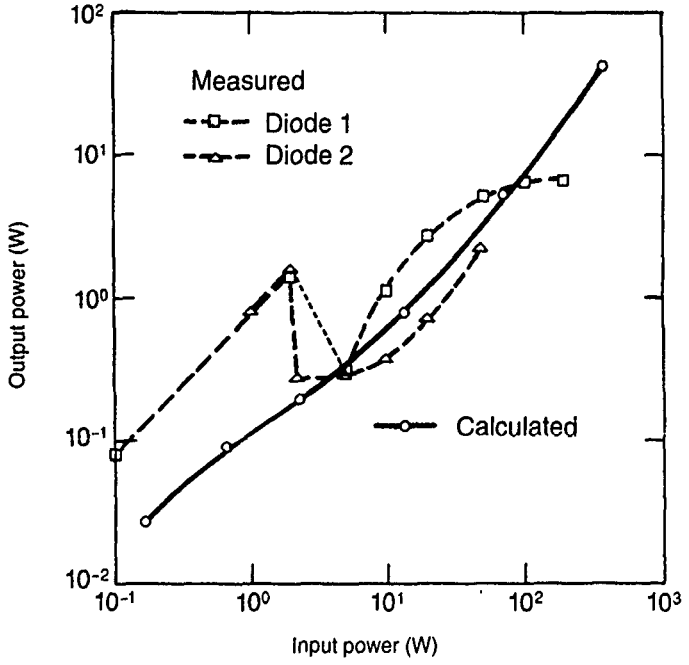


Figure 50. Comparison of calculated output power as a function of input power with measured curves for two 10-μm diodes at 1.5 GHz.

8. Damage Thresholds

Limiters primarily protect sensitive electronics from excessive rf power by the absorption or reflection of most of that power. If the power absorbed by the limiter is excessive, the limiter will be damaged. A damaged limiter may or may not continue to give protection, but almost certainly will prevent normal operation of a circuit. Manufacturers usually will give a safe operation range for cw operation, and some give some information for repetitive pulse operation in the microsecond pulsewidth range. In this section we consider damage threshold for single pulse exposure for pulsewidths in the nanosecond range.

8.1 Calculation Methodology

It is not feasible to extend calculations to the times required for sufficient heating to cause diode damage. Therefore, the heating rate at each specified power was used to extrapolate and obtain the predicted time to attain a specified temperature. An average temperature rise of 350 K (from the 300-K room temperature) had previously been found to correspond to dc second breakdown for the IN4148 [7]. However, since PIN diodes have little negative resistance, it is believed that a higher temperature would be required for damage of a PIN limiter. In this report, a rise of 500 K was usually chosen for the damage threshold. Calculations of heating caused by video (dc) pulses were also made and were compared with the results for the rf calculations.

Relaxation oscillations [7] were calculated when the reverse diode voltage exceeded the avalanche breakdown voltage. Figure 51 shows temporal current, voltage, and temperature curves for the reverse half-cycle calculated for a 1-μm diode at 2 GHz. The maximum applied voltage was 200 V, and two current spikes are noted. The dc avalanche voltage for a 1-μm PIN diode is 35 V, but an overvoltage is required for avalanching with rf excitation. The dynamic current-voltage characteristic for this calculation is shown in figure 52. The breakdown (maximum) voltage of the second cycle is lower than the first since a lower multiplication factor is required for the higher initiating current [7]. At higher applied rf voltages, additional relaxation cycles appear. Figure 53, calculated for 1000 V, shows that the oscillations are decaying rapidly and that the heating rate becomes nearly constant over most of the half cycle. Figure 54 shows the dynamic current-voltage characteristic for the higher power calculation. The 1-μm diode showed the strongest oscillations of the various diode widths used in the calculations.

Heating rate calculations made with initial temperatures of 400 and 500 K showed only a very small decrease in heating rates at these temperatures. Since the total current density in a one- dimensional diode is constant across the diode, heating will be proportional to the electric field. Under forward bias the electric field is greater at the center of the diode; hence the temperature curve has a maximum there. The temperature distribution across a diode after a forward half-cycle is shown in figure 55. With reverse bias, the maximum fields are at the PI and IN junctions; the temperature distribution

Figure 51. Relaxation oscillations and heating curve for reverse half-cycle at 200 V. Arrows indicate end of applied voltage half-cycle.

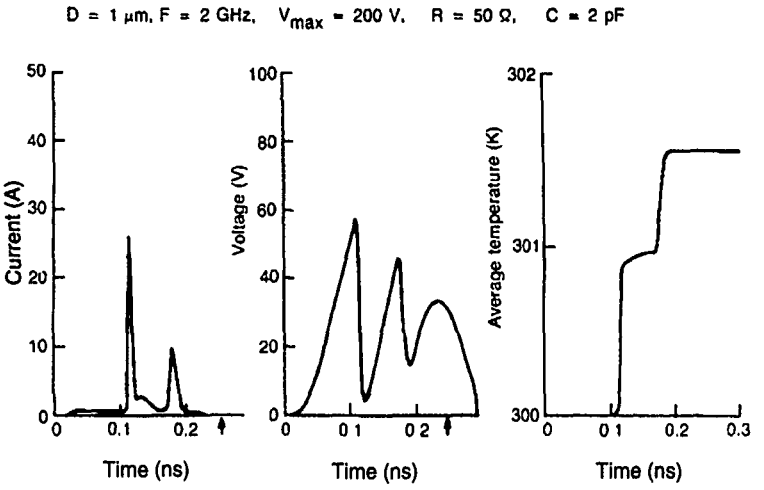


Figure 52. Dynamic characteristic for relaxation oscillations shown in figure 51.

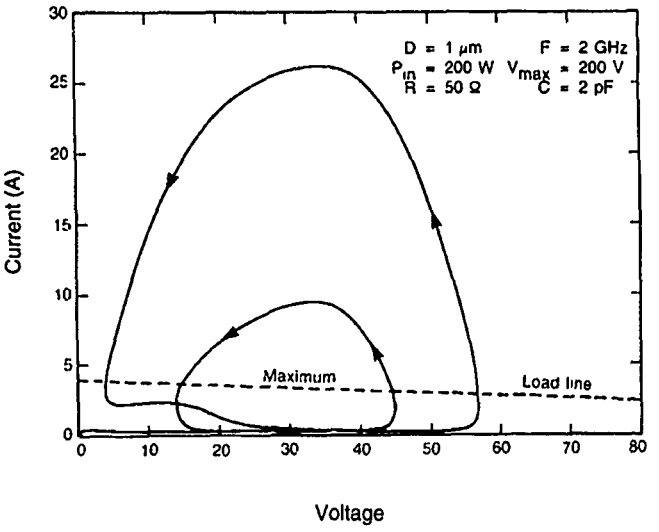
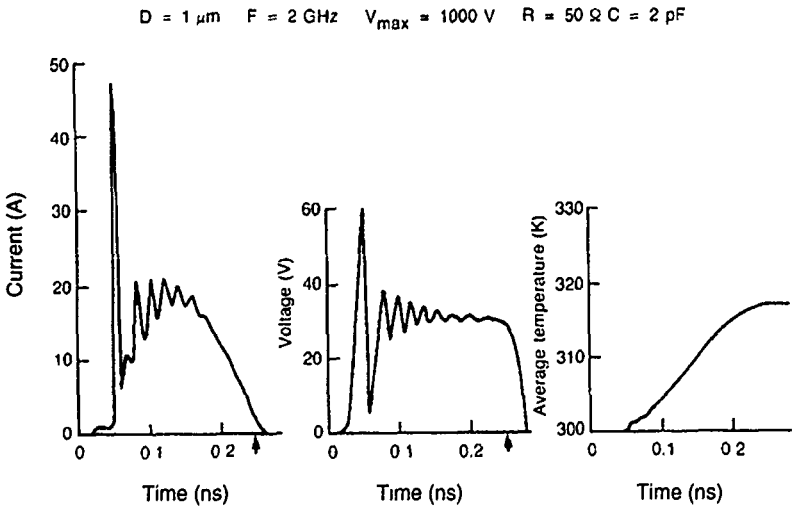
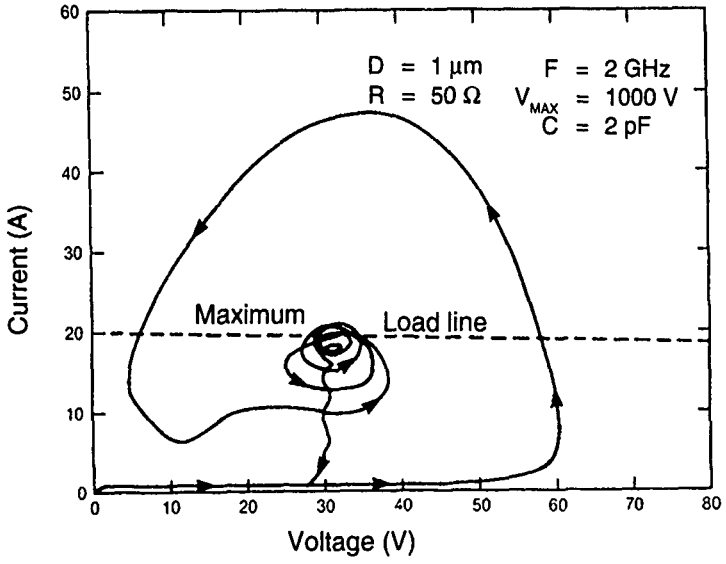


Figure 53. Relaxation oscillations and heating curve for reverse half-cycle at 1000 V. Arrows indicate end of applied voltage half-cycle.



thus has two peaks. Figure 56 depicts the temperature distribution after a reverse half-cycle. The temperatures shown in figures 51 and 53 are the average temperature across the diode. Since maximum heating occurs in different parts of the diode in the forward and reverse half-cycles, a more uniform temperature can be expected in rf excitation than for a dc reverse bias application. This indicates that a higher temperature peak would occur under dc conditions than for rf excitation at the same average temperature. Since damage occurs at the temperature maximum, a higher average temperature is expected for the damage thresholds with rf excitation than for a dc reverse bias. Previous calculations [7] showed that the heating rate was little changed when an actual computed temperature distribution was used as initial conditions rather than the same constant average temperature.

Figure 54. Dynamic characteristic of oscillations shown in figure 53.



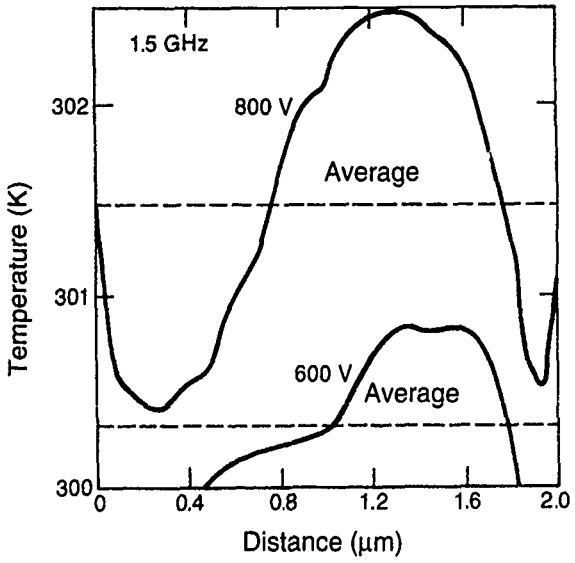


Figure 55. Temperature distribution at end of forward half-cycle at 1.5 GHz. Parameter is maximum voltage of applied waveform.

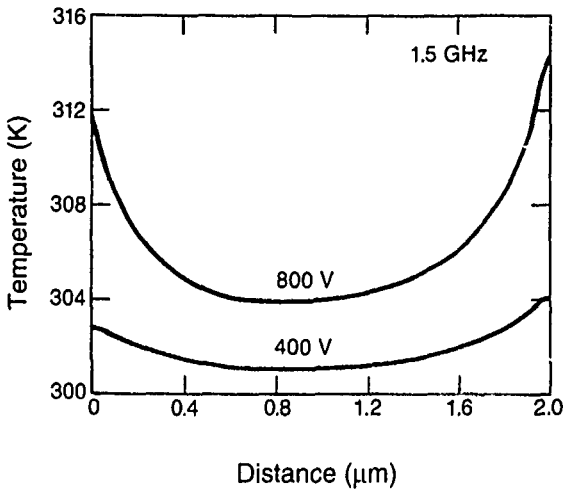


Figure 56. Temperature distribution at end of reverse half-cycle at 1.5 GHz. Parameter is maximum voltage of applied waveform.

8.2 Calculations of Damage Thresholds

Input power damage thresholds have been calculated for a 1-μm PIN diode at frequencies from 0.5 to 2.0 GHz. The results are shown in figure 57. The variation of the threshold with frequency in the calculated range is very small for the 1-μm PIN diode. The heating rate was also calculated for various applied dc reverse biases, and the time to reach 650 K (i.e., pulse length for damage) was obtained by the extrapolation. The dc results for the power dissipated by the diode are also shown in figure 57. The dc damage threshold is as much as an order of magnitude lower than the rf threshold. However, the dc threshold is for the actual power dissipated by the diode, whereas the rf power is the input power to the diode. When the power dissipated by the 50-Ω series resistor is included, the total dc input power is calculated to be nearly equal to the rf input power at the shorter pulse lengths.

8.3 Variation with Diode Width

Measured threshold damage power levels have shown a strong dependence on the width (thickness) of the intrinsic region of the PIN diode. Results of the calculated input-power damage thresholds for diodes of varying widths are shown in figure 58 as a function of pulse length (time for a temperature rise of 500 K). The rf frequency is 1.5 GHz. The temperature rise used in figure 57 was 350 K, whereas for figure 58 it was 500 K. Also, the formula for obtaining the input power from the applied voltage in figure 57 was slightly different from that used in figure 58. Therefore, the data for the two figures are not directly comparable.

Figure 58 shows that the damage threshold power decreases roughly linearly with pulse length; that is, approximately constant energy is required for damage. A constant energy curve is shown in figure 58 for reference. A

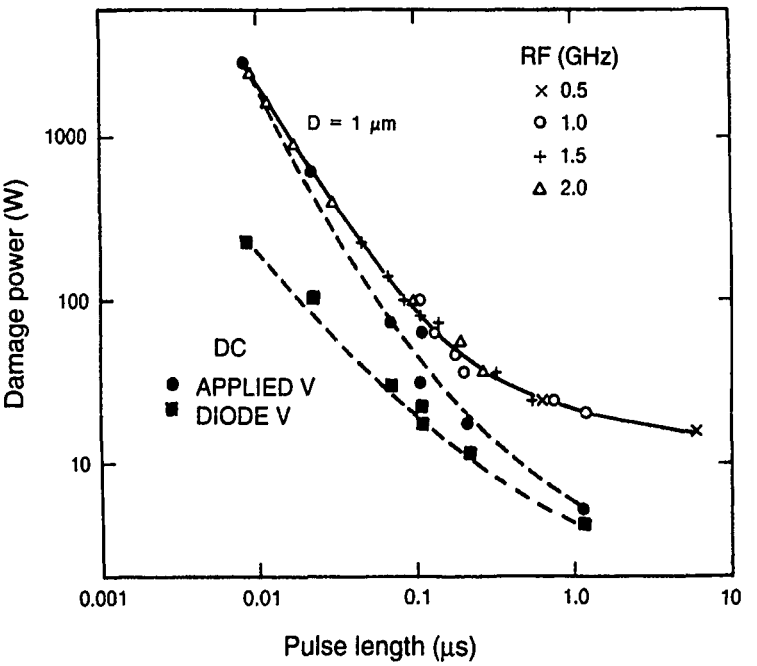


Figure 57. Calculated single-pulse damage thresholds for 1-μm diode as a function of pulse length.

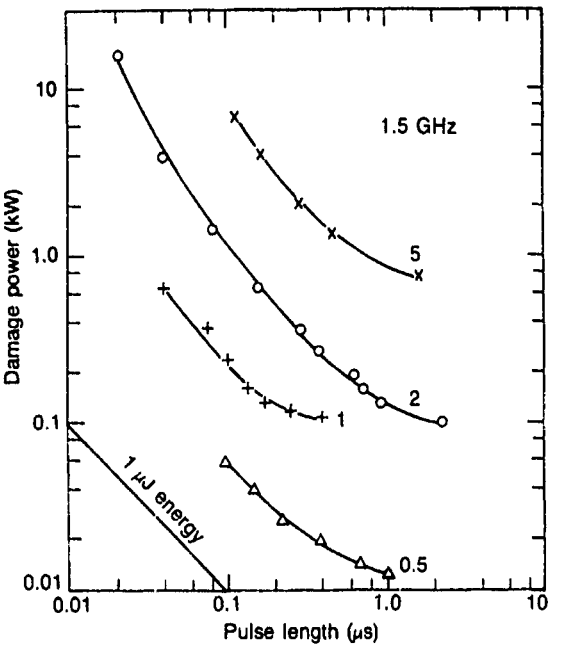


Figure 58. Calculated single-pulse damage thresholds for diodes of various widths as a function of pulse length. Parameter is diode width in micrometers. A constant energy curve is also shown.

closer look shows that at pulse lengths shorter than about 100 ns, the calculated damage power is increasing faster than linearly; therefore, the energy threshold is increasing. This increase is mainly attributed to greater reflected power from the highly conducting diodes. Some measured data support this increase. For pulse lengths greater than 1 μs the threshold power starts to level off. Calculations for pulse lengths greater than 1 μs are not considered as accurate and also will depend on the thermal time constant of the device. Because of a glitch in converting the computer program from card input to time sharing, heating rates of less than 1 K per nanosecond are set equal to zero. This circumstance is thought to approximately compensate for neglect of heat conduction in DIODE.

The calculated damage threshold power for a 0.1-μs pulse length is plotted as a function of diode width in figure 59. The slope of the straight line is 2.2, showing an increase with diode width slightly greater than the increase in volume of the diode. The areas of the devices were made proportional to widths, keeping the junction capacitance constant. The pulse length of 0.1 μs was chosen for the plot of figure 59 because it was the shortest pulse length which included all diode width calculations. Measurements of damage thresholds have been made for diodes of various widths with various pulse lengths. The results are shown in figure 60. The threshold power is about an order of magnitude greater but because of the shorter pulse length, the threshold energy is in reasonable agreement, as are the measured and calculated slopes. Later measurements have yielded a shallower slope, especially for thinner diodes.

8.4 Direct Comparison of Measured and Calculated Thresholds

The measured damage thresholds were obtained by step stressing the diode, usually doubling the power at a constant pulse length, but sometimes doubling the pulse length at a constant power. The criterion for damage was a definite lowering of the diode reverse-breakdown voltage. Usually a

Figure 59. Calculated variation of single-pulse damage thresholds as a function of diode width for 0.1-μs pulse.

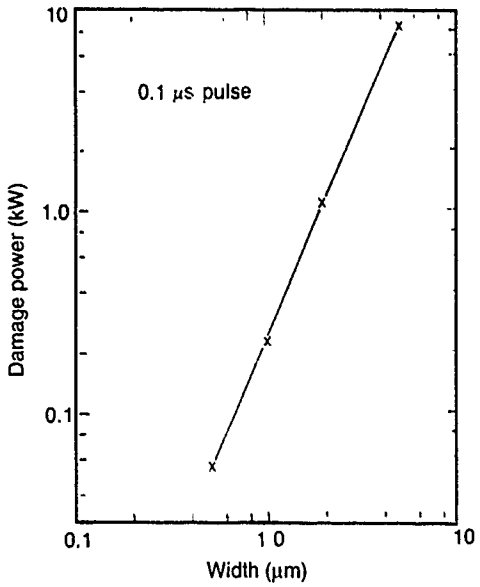
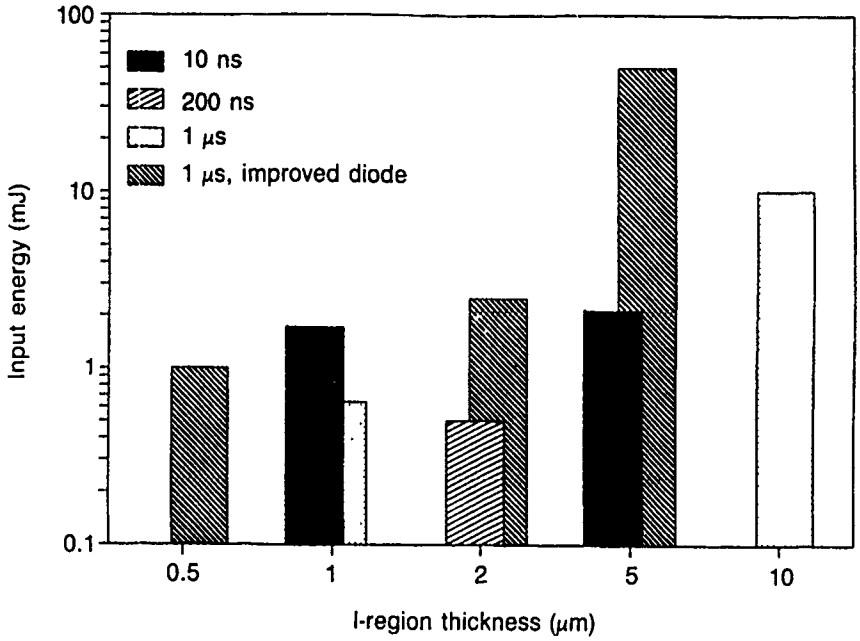


Figure 60. Measured energy damage thresholds for various I-region thicknesses and pulse lengths.



higher power was required to cause an increase in the insertion loss. The measured damage thresholds for two 2-μm diodes are shown in figure 61. Two points are shown for each diode; the diode survived the lower energy but failed at the higher energy. Also shown in this figure are the results of calculations for a 2-μm diode at the same frequencies. The agreement between the measured and calculated thresholds is satisfactory. The calculated thresholds show a greater frequency dependence at the longer pulse lengths than was noted for the 1-μm diode in figure 57. Longer pulse lengths entail operation near the avalanche threshold where the formative time lag for the avalanche to grow requires higher breakdown voltages at higher frequencies. This is essentially a transit-time phenomenon which is more evident for wider diodes. This trend is supported by limited calculations for wider diodes.

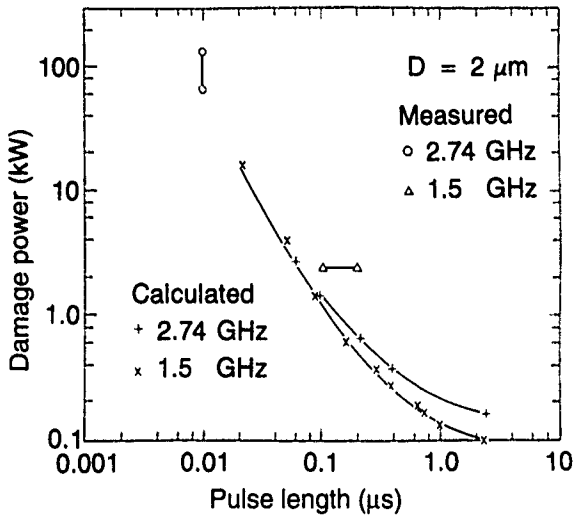


Figure 61. Comparison of measured and calculated damage thresholds for 2-μm diodes; experimental no-damage and damage points are shown.

It was shown in figure 41 that the energy absorbed and reflected by the diode increased sharply above the threshold for avalanching. In all the damage threshold calculations, avalanching is calculated during the reverse half-cycle and, above the avalanche threshold, the reverse-bias half-cycle power absorbed greatly exceeds that produced in the forward half-cycle. However, with sufficient stored charges, the avalanche voltage may not be attained. This is a plausible explanation of why diodes with superior isolation usually have a higher damage threshold. Alternatively, the greater reflectivity of the diode with superior isolation may be sufficient to explain the lower absorbed energy.

It is interesting to note that avalanching may be calculated during a forward half-cycle simulation at about one-half the reverse breakdown voltage [7]. However, the higher current due to avalanching is offset by the reduced voltage so there is little effect on the absorbed power. Further effort will be required to determine the effect of avalanching upon damage thresholds.

9. Further Discussion

The five preceding sections have discussed, in order, dc forward bias switching, forward biased conductivity, spike leakage, isolation, and damage thresholds. The emphasis has been on the results of computer simulations and their comparison with measured results. In all cases there is sufficient agreement to show that the computer model is basically accurate, but enough disagreement to demonstrate some inadequacies of the DIODE program. A consistent discrepancy is that DIODE predicts a faster initial current buildup upon application of either a forward dc bias or an unbiased or forward-biased rf signal. This was seen directly in figure 15(b) for the forward-biased rf signal and was seen consistently for the dc-biased transient. It is seen indirectly in the unbiased rf isolation calculations where the threshold input power for limiting is higher for the measured data than for the calculated. We return to this point below.

As postulated in section 5, we believe that the inadequate initial and boundary conditions used in our DIODE calculations are the cause of the calculated faster buildup. DIODE was designed to be used for reverse avalanche breakdown and not for low-current conditions. First, diffusion currents dominate at low currents and DIODE only calculates diffusion currents indirectly. Second, negative fields are always present at low currents and DIODE tends to be unstable with negative fields. Further, high doping levels at the P and N region boundaries are required for calculating accurate unbiased (zero current) initial charge distributions. High doping levels lead to short dielectric relaxation times, t_D. For example, for an electron density of 1×10^{17} cm^{-3} in silicon, $t_D = 3 \times 10^{-14}$ s. Since computer time steps of greater than t_D are potentially unstable, computer calculations at high doping levels become prohibitively expensive over problem times of interest. Despite these limitations meaningful calculations have been made. For practical purposes, the discrepancy in the initial phase of the current buildup is not important since its duration is typically only a couple of nanoseconds. In fact, the discrepancy was noted only with fast-rising experimental pulses.

While it has been generally assumed that the computer simulations must agree with the measurements, the latter are also subject to limitations and errors. In many cases where disagreement has been noted, changes in the experimental technique, for example, faster rising applied pulses, have brought the measured results into agreement with the calculated results.

Hori et al [18] from Toshiba reported results of measurements on high-power microwave integrated circuit (MIC) silicon limiters for S- and X-band radars. Their I-layer widths were 1.5, 5.5, 9.5, and 13.6 μm. Their measurements were made with 1-μs pulse widths and with a 0.1-percent duty cycle. They plotted average leakage power as a function of input power at 3 GHz. Each of the three widest diodes showed discontinuities in the average leakage power, while the 1.5-μm diode did not. This diode width dependence of the discontinuities is in good agreement with our measurements (sect. 7), in which diodes of 2-μm widths, or less, showed no discontinuity, while those of 5-μm widths, or greater, showed discontinuities. However, there is greater than an order of magnitude difference in the input and leakage power at which the discontinuities are noted. One difference is that Toshiba plotted average power for 1-μm pulses, whereas we plotted the flat leakage power, not an average of spike and flat leakage. Also, our discontinuities occur at the initiation of limiting, whereas Toshiba's discontinuities followed an isolation of as much as 10 dB. In investigating the discontinuity of their 9.5-μm diode, Hori et al showed that a sharp drop in leakage power, with a concurrent increase in rectified current, occurred at midpulse for an input power that was at the midpoint of their discontinuity. With further increase in input power, they state that "leakage power is only observed as a spike waveform in the front edge of the rf pulse." They make no mention of any spike leakage before the discontinuity.

One plausible explanation of the Toshiba discontinuity that can be deduced from our calculations is that it marks the onset of stored charges at the end of the reverse half-cycle. Computer calculations predict a maximum of about 10-dB isolation without stored charges remaining after the forward half-cycle, and a couple orders of magnitude more with stored charges.

Toshiba also used a network analyzer to measure the large-signal diode impedance of the 1.5- and 9.5-μm diodes, with both rf and forward-bias voltage. The impedance loci agreed well for the two excitations up to the maximum rf power usable. Their results show the 9.5-μm diode impedance with a forward bias traversing near the center of the Smith chart as the power increased to that corresponding to the discontinuity input power of the diode. The impedance locus of the 1.5-μm diode, in contrast, was found to lie on an almost constant reflection circle. They give this as a probable explanation of the presence of a discontinuity for the wider diode (no reflection at the center of the Smith chart) and the absence of the discontinuity for the narrow diode. They also mention thermal effects as an alternate explanation of the discontinuities.

Also note that Toshiba's Smith chart measurements were for equilibrium conditions and thus not directly comparable to our switching calculations shown in figure 18.

Kurata [19] has made a computer study of power-limiter diode behavior similar to this study. He made calculations for diodes of 0.5-, 1.0-, and 2.0-μm widths at a frequency of about 10 GHz. His source voltage amplitude varied from 1 to 900 V, and his line and load impedances were both 400 Ω. Overall, his calculated voltage waveforms are similar to those shown in this report. He also compared his calculated plots of output power as a function of input power with measurements made in his laboratory for diode widths of 0.5, 0.77, and 1.62 μm. His measurements showed fairly flat plateaus for input powers in the range of from about 1 to 30 W. His calculations show almost constant isolation in this power range. Also, the variation of output power with diode width was much greater for his calculations than for the measurements. Kurata attributes his failure to calculate the measured plateaus to the inadequacy of his external circuit. He obtained a short plateau by adding a small inductance parallel to his diode in his calculations. Kurata also found a flattening of the output power due to avalanching at several hundred watts of input power. This is in satisfactory agreement with our calculations (see fig. 41).

10. Conclusions and Future Work

10.1 Conclusions

A combined theoretical and experimental study of spike leakage and burnout has been made for silicon PIN diodes exposed to short, single-pulse excitation. The diodes ranged in intrinsic-level thickness from 0.5 to 50 μm. Diodes of 2-μm thickness, or less, showed little spike leakage but were damaged at lower input power than diodes of 5-μm thickness or greater. The thicker diodes had considerable spike leakage, which could damage sensitive electronics. The computer studies showed that the spike leakage was determined by a complex interaction of transit-time effects, stored charges from forward conduction and space charge effects during reverse conduc-

tion. Burnout threshold powers are higher for thicker diodes as a result of their higher avalanche breakdown voltages and because of their larger volume.

Supporting our studies of spike leakage and burnout are studies of dc transients and the forward-biased rf conductivity of PIN diodes. There are fewer limitations on the computer simulation of these latter studies, and comparisons with measurements are more complete. In all cases, the comparison of computed and measured voltage and current waveforms has contributed the most to our understanding of spike leakage and burnout. The waveform studies also point to the importance of the external circuit in the limiter's performance. In particular, the effect of a series inductance (as from the diode leads, packaging, or probes) was simulated in good agreement with measured waveforms.

Experimental measurements of the wider diodes with large spike leakage showed a discontinuity in isolation at a threshold input power. At the same threshold the diodes under cw excitation showed the discontinuity and a hysteresis, in that limiting continued at lower input powers than the initial threshold.

10.2 Future Work

Our future work on PIN diode limiters will be guided largely by a cooperative research and development agreement (CRDA) recently signed with a commercial device manufacturer. This manufacturer will supply HDL with PIN diodes. The initial diodes will be 5-μm silicon, but GaAs diodes will be supplied later. The diode's doping profile (P-ν-N) and cross-sectional area will be known and compared with DIODE to allow comparison of the voltage and current waveforms. If possible, P-π-N diodes will be fabricated and tested to determine if they are faster because of the presence of background holes in the intrinsic region. In cooperation with the manufacturer, HDL will make laboratory measurements of spike leakage, flat leakage, and damage thresholds and perform the DIODE simulations.

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